



***GE Solid State***

**DATABOOK**

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## **RCA Advanced CMOS Logic ICs**



**54/74AC and 54/74ACT SERIES**

# RCA Advanced CMOS Logic Integrated Circuits

The RCA AC/ACT series of Advanced CMOS Logic (ACL) integrated circuits include a broad line of products that match bipolar FAST\* products in speed, performance, and logic-type output drive, but at CMOS power levels. The product line consists of CD54/74AC-series types, which feature CMOS input-voltage-level compatibility, and CD54/74ACT-series types, which are input-voltage-level-compatible with LSTTL devices. Because of its low power consumption, ACL is more reliable than bipolar logic. This quality should make ACL the technology of choice in a number of applications, including computers, peripherals, and telecommunications, and in portable and military equipment.

Featuring <3-ns propagation delays for gate products, ACL is the fastest complete CMOS logic family yet available. (By contrast, the standard propagation delay for CMOS logic is 95 ns, and for high-speed CMOS logic, 9 ns.) ACL can operate at more than 150 MHz. Output drive capability is 24 mA, compared with 6 mA for HC/HCT. This capability enables ACL to drive transmission lines, yet still generate the voltages necessary to operate the receiving logic devices safely.

Other key family features of the RCA ACL line include:

- ESD protection in excess of 2kV - MIL-STD-883, Method 3015
- SCR-latch-up-resistant CMOS process and circuit design
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- Reduced switching transient ("ground bounce") effects

With the broad line of CMOS CD4000-series types currently available, together with performance offered by the RCA HC/HCT series of high-speed CMOS ICs and the RCA AC/ACT series of advanced high-speed CMOS logic ICs, the designer need not sacrifice speed for power consumption. Add the other classical advantages of CMOS, including high noise immunity and wide power supply and temperature ranges, and the decision to use CMOS logic is the choice. This family provides for the design of more cost-effective systems to serve high-speed market applications.

\*FAST is a Trademark of Fairchild Semiconductor Corp.

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The device data shown for some types are indicated as product preview or advance information data. Product preview data are intended for engineering evaluation of product under development. The type designations and data are subject to change or withdrawal, unless otherwise arranged. Advance information data are intended for guidance purposes in evaluating new product for

equipment design. Such data are shown for types currently being designed for inclusion in our standard line of commercially available products. No obligations are assumed for notice of change or these devices. For current information on the status of product preview or advance information data programs, please contact your local GE Solid State sales office.

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CD74AC02E/M	CD54AC02F	CD74ACT02E/M	CD54ACT02F	52	Quad 2-Input NOR Gate	14
CD74AC04E/M	CD54AC04F	CD74ACT04E/M	CD54ACT04F	56	Hex Inverter/Buffer	14
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CD74AC32E/M	CD54AC32F	CD74ACT32E/M	CD54ACT32F	75	Quad 2-Input OR Gate	14
CD74AC74E/M	CD54AC74F	CD74ACT74E/M	CD54ACT74F	79	Dual D Flip-Flop w/Set and Reset	14
CD74AC86E/M	CD54AC86F	CD74ACT86E/M	CD54ACT86F	85	Quad 2-Input Exclusive-OR Gate	14
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†Package Suffix E - Dual-In-Line Plastic EN - Dual-In-Line Narrow-Body Plastic F - Dual-In-Line Frit-Seal Ceramic M - Small Outline						



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<b>Bus Transceivers</b>			
AC/ACT245	Octal-Bus Transceiver; 3-State	MSI	176
AC/ACT623	Octal-Bus Transceiver; 3-State	MSI	256
AC/ACT646	Octal-Bus Transceiver/Register; 3-State	MSI	262
AC/ACT647	Octal-Bus Transceiver/Register with Open Drain	MSI	269
AC/ACT648	Octal-Bus Transceiver/Register; 3-State; Inverting	MSI	262
AC/ACT649	Octal-Bus Transceiver/Register with Open Drain; Inverting	MSI	269
AC/ACT651	Octal-Bus Transceiver/Register; 3-State; Inverting	MSI	276
AC/ACT652	Octal-Bus Transceiver/Register; 3-State	MSI	276
AC/ACT653	Octal-Bus Transceiver/Register; Open-Drain (A Side); 3-State (B Side); Inverting	MSI	283
AC/ACT654	Octal-Bus Transceiver/Register; Open-Drain (A Side) 3-State (B-Side)	MSI	283
AC/ACT7623	Octal-Bus Transceiver; 3-State (B Side); Open-Drain (A Side)	MSI	294
<b>Schmitt Trigger</b>			
AC/ACT14	Hex Inverting Schmitt Trigger	SSI	69
<b>Latches</b>			
AC/ACT373	Octal Transparent Latch; 3-State	MSI	222
AC/ACT533	Octal Transparent Latch; 3-State; Inverting	MSI	222
AC/ACT563	Octal Transparent Latch; 3-State; Inverting	MSI	242
AC/ACT573	Octal Transparent Latch; 3-State	MSI	242

- Open Drain (one side)

## Cross-Reference Guide

Industry Type	RCA Replacement Type	Industry Type	RCA Replacement Type	Industry Type	RCA Replacement Type
54AC00D	CD54AC00F	74AC00P	CD74AC00E	74AC00S	CD74AC00M
54AC02D	CD54AC02F	74AC02P	CD74AC02E	74AC02S	CD74AC02M
54AC04D	CD54AC04F	74AC04P	CD74AC04E	74AC04S	CD74AC04M
54AC05D	CD54AC05F	74AC05P	CD74AC05E	74AC05S	CD74AC05M
54AC08D	CD54AC08F	74AC08P	CD74AC08E	74AC08S	CD74AC08M
54AC10D	CD54AC10F	74AC10P	CD74AC10E	74AC10S	CD74AC10M
54AC14D	CD54AC14F	74AC14P	CD74AC14E	74AC14S	CD74AC14M
54AC20D	CD54AC20F	74AC20P	CD74AC20E	74AC20S	CD74AC20M
54AC32D	CD54AC32F	74AC32P	CD74AC32E	74AC32S	CD74AC32M
54AC74D	CD54AC74F	74AC74P	CD74AC74E	74AC74S	CD74AC74M
54AC86D	CD54AC86F	74AC86P	CD74AC86E	74AC86S	CD74AC86M
54AC109D	CD54AC109F	74AC109P	CD74AC109E	74AC109S	CD74AC109M
54AC112D	CD54AC112F	74AC112P	CD74AC112E	74AC112S	CD74AC112M
54AC138D	CD54AC138F	74AC138P	CD74AC138E	74AC138S	CD74AC138M
54AC139D	CD54AC139F	74AC139P	CD74AC139E	74AC139S	CD74AC139M
54AC151D	CD54AC151F	74AC151P	CD74AC151E	74AC151S	CD74AC151M
54AC153D	CD54AC153F	74AC153P	CD74AC153E	74AC153S	CD74AC153M
54AC157D	CD54AC157F	74AC157P	CD74AC157E	74AC157S	CD74AC157M
54AC158D	CD54AC158F	74AC158P	CD74AC158E	74AC158S	CD74AC158M
54AC161D	CD54AC161F	74AC161P	CD74AC161E	74AC161S	CD74AC161M
54AC163D	CD54AC163F	74AC163P	CD74AC163E	74AC163S	CD74AC163M
54AC164D	CD54AC164F	74AC164P	CD74AC164E	74AC164S	CD74AC164M
54AC174D	CD54AC174F	74AC174P	CD74AC174E	74AC174S	CD74AC174M
54AC175D	CD54AC175F	74AC175P	CD74AC175E	74AC175S	CD74AC175M
54AC191D	CD54AC191F	74AC191P	CD74AC191E	74AC191S	CD74AC191M
54AC193D	CD54AC193F	74AC193P	CD74AC193E	74AC193S	CD74AC193M
54AC238D	CD54AC238F	74AC238P	CD74AC238E	74AC238S	CD74AC238M
54AC240D	CD54AC240F	74AC240P	CD74AC240E	74AC240S	CD74AC240M
54AC241D	CD54AC241F	74AC241P	CD74AC241E	74AC241S	CD74AC241M
54AC244D	CD54AC244F	74AC244P	CD74AC244E	74AC244S	CD74AC244M
54AC245D	CD54AC245F	74AC245P	CD74AC245E	74AC245S	CD74AC245M
54AC251D	CD54AC251F	74AC251P	CD74AC251E	74AC251S	CD74AC251M
54AC253D	CD54AC253F	74AC253P	CD74AC253E	74AC253S	CD74AC253M
54AC257D	CD54AC257F	74AC257P	CD74AC257E	74AC257S	CD74AC257M
54AC258D	CD54AC258F	74AC258P	CD74AC258E	74AC258S	CD74AC258M
54AC273D	CD54AC273F	74AC273P	CD74AC273E	74AC273S	CD74AC273M
54AC280D	CD54AC280F	74AC280P	CD74AC280E	74AC280S	CD74AC280M
54AC283D	CD54AC283F	74AC283P	CD74AC283E	74AC283S	CD74AC283M
54AC299D	CD54AC299F	74AC299P	CD74AC299E	74AC299S	CD74AC299M
54AC323D	CD54AC323F	74AC323P	CD74AC323E	74AC323S	CD74AC323M
54AC373D	CD54AC373F	74AC373P	CD74AC373E	74AC373S	CD74AC373M
54AC374D	CD54AC374F	74AC374P	CD74AC374E	74AC374S	CD74AC374M
54AC533D	CD54AC533F	74AC533P	CD74AC533E	74AC533S	CD74AC533M
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54AC541D	CD54AC541F	74AC541P	CD74AC541E	74AC541S	CD74AC541M
54AC563D	CD54AC563F	74AC563P	CD74AC563E	74AC563S	CD74AC563M
54AC564D	CD54AC564F	74AC564P	CD74AC564E	74AC564S	CD74AC564M
54AC573D	CD54AC573F	74AC573P	CD74AC573E	74AC573S	CD74AC573M
54AC574D	CD54AC574F	74AC574P	CD74AC574E	74AC574S	CD74AC574M
54AC623D	CD54AC623F	74AC623P	CD74AC623E	74AC623S	CD74AC623M
54AC646D	CD54AC646F	74AC646P	CD74AC646EN	74AC646S	CD74AC646M
54AC647D	CD54AC647F	74AC647P	CD74AC647EN	74AC647S	CD74AC647M
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54AC654D	CD54AC654F	74AC654P	CD74AC654EN	74AC654S	CD74AC654M
54AC7060D	CD54AC7060F	74AC7060P	CD74AC7060E	74AC7060S	CD74AC7060M
54AC7201D	CD54AC7201F	74AC7201P	CD74AC7201E	74AC7201S	CD74AC7201M
54AC7202D	CD54AC7202F	74AC7202P	CD74AC7202E	74AC7202S	CD74AC7202M
54AC7623D	CD54AC7623F	74AC7623P	CD74AC7623E	74AC7623S	CD74AC7623M

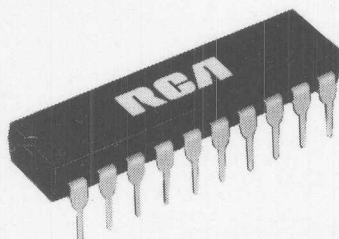


## Cross-Reference Guide

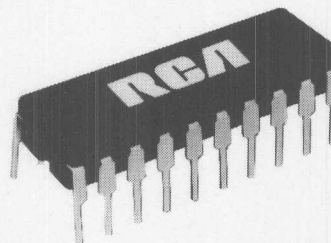
Industry Type	RCA Replacement Type	Industry Type	RCA Replacement Type	Industry Type	RCA Replacement Type
54ACT00D	CD54ACT00F	74ACT00P	CD74ACT00E	74ACT00S	CD74ACT00M
54ACT02D	CD54ACT02F	74ACT02P	CD74ACT02E	74ACT02S	CD74ACT02M
54ACT04D	CD54ACT04F	74ACT04P	CD74ACT04E	74ACT04S	CD74ACT04M
54ACT05D	CD54ACT05F	74ACT05P	CD74ACT05E	74ACT05S	CD74ACT05M
54ACT08D	CD54ACT08F	74ACT08P	CD74ACT08E	74ACT08S	CD74ACT08M
54ACT10D	CD54ACT10F	74ACT10P	CD74ACT10E	74ACT10S	CD74ACT10M
54ACT14D	CD54ACT14F	74ACT14P	CD74ACT14E	74ACT14S	CD74ACT14M
54ACT20D	CD54ACT20F	74ACT20P	CD74ACT20E	74ACT20S	CD74ACT20M
54ACT32D	CD54ACT32F	74ACT32P	CD74ACT32E	74ACT32S	CD74ACT32M
54ACT74D	CD54ACT74F	74ACT74P	CD74ACT74E	74ACT74S	CD74ACT74M
54ACT86D	CD54ACT86F	74ACT86P	CD74ACT86E	74ACT86S	CD74ACT86M
54ACT109D	CD54ACT109F	74ACT109P	CD74ACT109E	74ACT109S	CD74ACT109M
54ACT112D	CD54ACT112F	74ACT112P	CD74ACT112E	74ACT112S	CD74ACT112M
54ACT138D	CD54ACT138F	74ACT138P	CD74ACT138E	74ACT138S	CD74ACT138M
54ACT139D	CD54ACT139F	74ACT139P	CD74ACT139E	74ACT139S	CD74ACT139M
54ACT151D	CD54ACT151F	74ACT151P	CD74ACT151E	74ACT151S	CD74ACT151M
54ACT153D	CD54ACT153F	74ACT153P	CD74ACT153E	74ACT153S	CD74ACT153M
54ACT157D	CD54ACT157F	74ACT157P	CD74ACT157E	74ACT157S	CD74ACT157M
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54ACT161D	CD54ACT161F	74ACT161P	CD74ACT161E	74ACT161S	CD74ACT161M
54ACT163D	CD54ACT163F	74ACT163P	CD74ACT163E	74ACT163S	CD74ACT163M
54ACT164D	CD54ACT164F	74ACT164P	CD74ACT164E	74ACT164S	CD74ACT164M
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54ACT191D	CD54ACT191F	74ACT191P	CD74ACT191E	74ACT191S	CD74ACT191M
54ACT193D	CD54ACT193F	74ACT193P	CD74ACT193E	74ACT193S	CD74ACT193M
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54ACT273D	CD54ACT273F	74ACT273P	CD74ACT273E	74ACT273S	CD74ACT273M
54ACT280D	CD54ACT280F	74ACT280P	CD74ACT280E	74ACT280S	CD74ACT280M
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54ACT7060D	CD54ACT7060F	74ACT7060P	CD74ACT7060E	74ACT7060S	CD74ACT7060M
54ACT7201D	CD54ACT7201F	74ACT7201P	CD74ACT7201E	74ACT7201S	CD74ACT7201M
54ACT7202D	CD54ACT7202F	74ACT7202P	CD74ACT7202E	74ACT7202S	CD74ACT7202M
54ACT7623D	CD54ACT7623F	74ACT7623P	CD74ACT7623E	74ACT7623S	CD74ACT7623M

## Packages

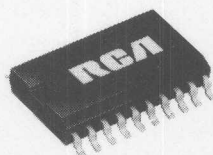
Typical Dual-In-Line  
Plastic Package



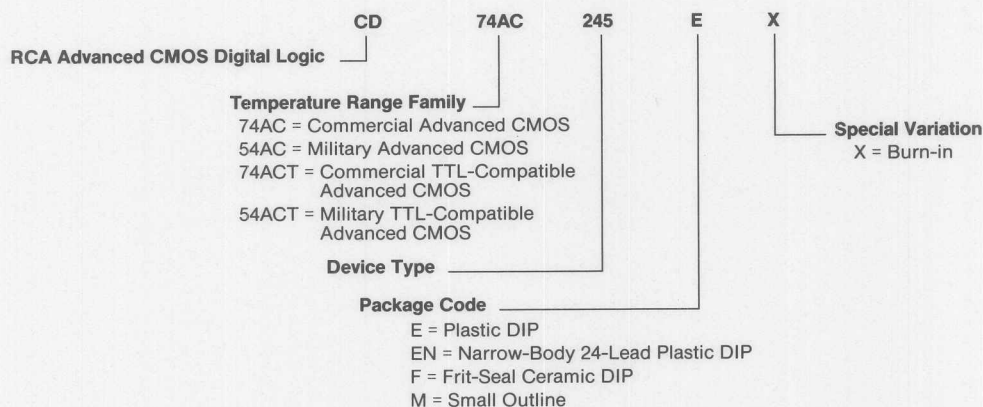
Typical Dual-In-Line  
Frit-Seal Ceramic (CERDIP) Package



Typical SO (Small Outline)  
Plastic Package



## Ordering Information



### Temperature Range

All packages when properly derated can be operated at 125°C.  
At low temperature, limit for E and M packages is -40°C, for F package, -55°C.

### Package Outlines

The package outlines indicated above are shown in the dimensional outlines section.

The package outlines indicated above are shown in the dimensional outlines section.

#### Package Outlines

All packages when properly derated can be operated at 125°C. At low temperature, limit for E and M packages is -40°C, for F package, -55°C.

#### Temperature Range

Package Code  
E = Plastic DIP  
EN = Narrow-Body 24-Lead Plastic DIP  
F = Pin-Grid Ceramic DIP  
M = Small Outline

#### Device Type

54ACT = Military TTL-Compatible Advanced CMOS

74ACT = Commercial TTL-Compatible Advanced CMOS

54AC = Military Advanced CMOS

74AC = Commercial Advanced CMOS

#### Temperature Range Family

CD = RCA Advanced CMOS Digital Logic

Package Code

54AC

54S

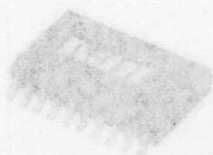
E

X

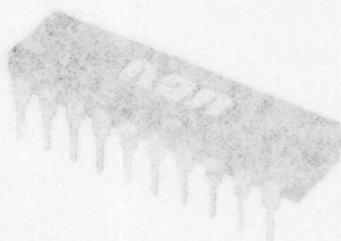
Special Variation  
X = Burn-in

## Ordering Information

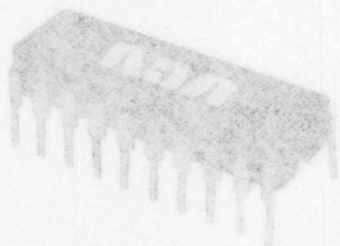
Typical 20 (Small Outline)  
Plastic Package



Typical Dual-In-Line  
Plastic Package



Typical Dual-In-Line  
Pin-Grid Ceramic (CERDIP) Package



## Packages

# Technical Overview

## FEATURES

The RCA ACL series of Advanced High-Speed CMOS integrated circuits is comprised of a broad range of logic types equivalent in performance and speed to FAST, AS (Advanced Schottky), and S (Schottky) bipolar types, but superior in that they require substantially less power in logic operations. Each CMOS circuit function is offered in two basic logic series, as follows:

1. CDBVACTXX-series types. These types feature TTL input-voltage-level compatibility and, using the same standardized pin-outs, provide reduced power-consumption alternatives to the very high power consumption of the FAST, AS, and S bipolar logic series types.
2. CDBVACTXX-series types. These types feature CMOS input-voltage-level compatibility and, using the same standardized pin-outs, provide enhanced system performance (better system noise margin) at speeds similar to those of FAST, AS, and S bipolar types.

The AACT family consists of a comprehensive set of octal buffers, octal latches, octal flip-flops, octal transceivers in both the classic 200-series pin-out and the newer 500-series flow-through pin-out. In addition, selected 251 inverters, gates, flip-flops, Schmitt triggers, plus selected MSI counters, registers, multiplexers, decoders, arithmetic functions, and FIFO's are included for a total of 63 circuits. In both the ACT and AC series, more types are planned.

Table 1. Performance Comparison of AACT and FAST Logic Functions

Characteristics		74 Series AACT		74 Series FAST	
1. Power Consumption (mW):	Four-stage counter (191)	0.44	5.5	0	1
	Octal transceiver (245)	0.44	39	489	308
2. Operating Voltage (volts):		ACT: 4.5 to 5.5 AC: 1.5 to 5.5		4.75 to 5.25	
3. Operating Temperature Range (°C):		-40 to +125		0 to +70	
4. Noise Margin (volts):	(V <sub>cc</sub> =4.5 V, rated load)	1.52/1.25		0.4/0.3	
	FAST to FAST AC to AC (High/Low) ACT to ACT	1.6/0.38		---	
5. Input Switching Voltage Variation over the Operating Temperature Range (mV):		V <sub>s</sub> ± 50		V <sub>s</sub> ± 500	
6. Output Drive Current (mA):	Bus Drivers	±24		+84/-18	
	3-State Buffers 251 MSI Logic (V <sub>cc</sub> =4.5 V)	±24		+20/-1 (Low)	
7. Propagation Delay (ns):	Octal Buffer (240)	7.0/7.8		6.9	
	Flip-Flop (74)	9.4/9.4		10.5/9.5	
8. Input Current (μA):	I <sub>l</sub>	+1		+1800	
	I <sub>h</sub>	-1		-30	
9. Three-State Output Current (μA):		±5		±50	

## ACL Family Features

- Following is a listing of the features of the ACL family of logic devices.
- Functionally and pin-compatible with industry 64 and 74 bipolar types in the FAST, AS, and S series
  - CMOS rail-to-rail output swing for maximum noise margins
  - Fanout (over temperature):  
2400 ACL Loads  
18 FAST Loads  
48 AS Loads
  - Wide operating-temperature ranges:  
Plastic (DIP) and Small-Outline 74 series: -40 to +125°C  
Ceramic (GEOIP) 64 series: -55 to +125°C
- NOTE: FAST, AS, and S series types are rated for only 0 to +70°C
- Balanced propagation and output transition times
  - Improved equipment reliability in improved equipment reliability
  - Outputs readily drive 80-ohm lines (74 series) and 75-ohm lines (64 series) without need for terminations
  - Meets JEDEC Standard No. 20; presently, in draft (non-issued) form
  - Octal types have typically a 1-volt peak simultaneous switching-voltage transient, similar to FAST series
  - CMOS input compatible



## FEATURES

The RCA ACL series of Advanced High-Speed CMOS Integrated Circuits is comprised of a broad range of logic types equivalent in performance and speed to FAST, AS (Advanced Schottky), and S (Schottky) bipolar types, but superior in that they require substantially less power in logic operations. Each CMOS circuit function is offered in two basic logic series, as follows:

1. **CD54/74ACTXXX-series types.** These types feature TTL input-voltage-level compatibility and, using the same standardized pin-outs, provide reduced power-consumption alternatives to the very high power consumption of the FAST, AS, and S bipolar logic series types.
2. **CD54/74ACXXX-series types.** These types feature CMOS input-voltage-level compatibility and, using the same standardized pin-outs, provide enhanced system performance (better system noise margin) at speeds similar to those of FAST, AS, and S logic series types.

The AC/ACT family consists of a comprehensive set of octal buffers, octal latches, octal flip-flops, octal transceivers in both the classic 200-series pin-out and the newer 500-series flow-through pin-out. In addition, selected SSI inverters, gates, flip-flops, Schmitt triggers, plus selected MSI counters, registers, multiplexers, decoders, arithmetic functions, and FIFO's are included for a total of 63 circuits, in both the ACT and AC series; more types are planned.

## ACL Family Features

Following is a listing of the features of the ACL family of logic devices.

- Functionally and pin-compatible with industry 54 and 74 bipolar types in the FAST, AS, and S series
- CMOS rail-to-rail output swing for maximum noise margins
- Fanout (over temperature):  
2400 ACL Loads  
15 FAST Loads  
48 AS Loads
- Wide operating-temperature ranges:  
Plastic (DIP) and Small-Outline 74 series: -40 to +125°C  
Ceramic (CERDIP) 54 series: -55 to +125°C  
NOTE: FAST, AS, and S series types are rated for only 0 to +70°C
- Balanced propagation and output transition times
- Significant power reduction compared to FAST, AS, and S TTL logic, resulting in improved equipment reliability
- Outputs reliably drive 50-ohm lines (74 series) and 75-ohm lines (54 series) without need for terminations
- Meets JEDEC Standard No. 20; presently, in draft (non-issued) form
- Octal types have typically a 1-volt peak simultaneous switching-voltage transient, similar to FAST series
- CMOS input compatible

Table I. Performance Comparison of AC/ACT and FAST Logic Functions.

Characteristic	74 Series AC/ACT			74 Series FAST		
<b>1. Power Consumption (mW):</b>	<b>Frequency (MHz)</b>			<b>Frequency (MHz)</b>		
	<b>0</b>	<b>1</b>	<b>10</b>	<b>0</b>	<b>1</b>	<b>10</b>
Four-stage counter (191)	0.44	5.5	55	204	224	306
Octal transceiver (245)	0.44	39	390	468	514	702
<b>2. Operating Voltage (volts):</b>	AC: 1.5 to 5.5 ACT: 4.5 to 5.5			4.75 to 5.25		
<b>3. Operating Temperature Range (°C):</b>	-40 to +125			0 to +70		
<b>4. Noise Margin (volts):</b> (V <sub>CC</sub> =4.5 V, rated load)				0.4/0.3		
FAST to FAST	—			—		
AC to AC (High/Low)	1.25/1.25			—		
ACT to ACT	1.8/0.36			—		
<b>5. Input Switching Voltage Variation over the Operating Temperature Range (mV):</b>	V <sub>S</sub> ± 50			V <sub>S</sub> ± 200		
<b>6. Output Drive Current (mA):</b> (V <sub>CC</sub> =4.5 V)				(I <sub>OL</sub> /I <sub>OH</sub> )		
SSI/MSI Logic	±24			+20/-1		
3-State Buffers	±24			+24/-3		
Bus Drivers	±24			+64/-15		
<b>7. Propagation Delay (ns):</b> (t <sub>PHL</sub> /t <sub>PLH</sub> )						
Octal Buffer (240)	7.8/7.8			6/9		
Flip-Flop (74)	9.4/9.4			10.5/8.5		
<b>8. Input Current (μA):</b>						
I <sub>IL</sub>	+1			+1600		
I <sub>IH</sub>	-1			-20		
<b>9. Three-State Output Current (μA):</b>	±5			±50		

### Series Features

Following are the special features of the AC series of Advanced CMOS High-Speed ICs.

- 1.5- to 5.5-volt operation
- High noise immunity:  
 $N_{IL} = N_{IH} = 30\%$  for  $V_{CC} = 3$  to 5 volts  
 $N_{IL} = N_{IH} = 20\%$  for  $V_{CC} = 1.5$  to 3 volts

Following are the special features of the ACT Series of Advanced CMOS High-Speed ICs.

- 4.5 to 5.5-volt operation
- Direct TTL input logic compatible:  
 $V_{IL} = 0.8$  volt (max);  $V_{IH} = 2$  volts (min)
- Similar to FAST specifications except for the 64 milliampere  $I_{OL}$  of FAST drivers

### Comparison of AC/ACT Logic Types with FAST/AS Types

RCA AC and ACT types have many outstanding advantages when compared with the conventional high-current bipolar FAST and AS logic types. The Advanced CMOS Logic AC and ACT types can replace the bipolar types in existing equipment and in new equipment designs requiring devices that operate at frequencies up to 100 MHz. Table I compares the significant operating characteristics of the AC and ACT CMOS types with those of the bipolar FAST logic family.

### ACL IC Process and Structure

Advanced CMOS high-speed products are fabricated with an advanced small-geometry CMOS process and design rules that are tailored to meet the specified high speed and high output-drive current, and to tame the high switching-current transients associated with high-speed designs. Fig. 1 shows the cross section of an AC/ACT chip. The starting material is a p-substrate topped with a thin p-epitaxial surface layer; hence, this process is an n-well type. The epitaxial surface serves essentially to eliminate SCR latch-up and provides for a low-impedance surface-conduction path that enhances electrostatic discharge capability. The n and p diffusions are ion-implanted. Polysilicon gates having an effective length of 1.5 microns are deposited over a thin 250-angstrom gate oxide. Active source and drain areas are automatically aligned to the separate gates with the polysilicon gates acting as a mask. This structure drastically

reduces the parasitic capacitances between the gate and the n and p areas (See Fig. 2) and, as a result, enhances switching speed. The n and p transistors are isolated by the areas of silicon dioxide, as shown in Fig. 1.

A major structural feature of AC/ACT devices is the use of two metallization levels. Logic interconnections are shorter because of the dual interconnect layers, and  $V_{CC}$  and ground distribution busing is greatly enhanced to handle the switching transient current, which can exceed one ampere for AC/ACT octal buffer types.

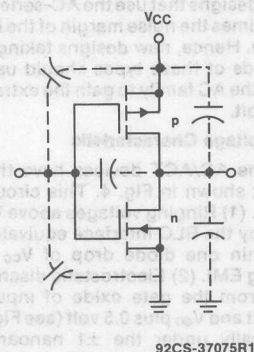


Fig. 2. Parasitic capacitances in a CMOS inverter.

### INPUT CHARACTERISTICS

The inputs of the ACL devices are sensitive to voltage levels. The only input current is the reverse diode leakage (a few picoamperes) of the protection network for electrostatic discharge. The definitive I/O switching characteristics of an input stage is shown in Fig. 3 (a) for AC types and in Fig. 3 (b) for ACT types. The specified MIN/MAX input switching voltages are guaranteed over the operating temperature range. Actual shift of the input voltage over the temperature range -55 to +125°C is 100 millivolts.

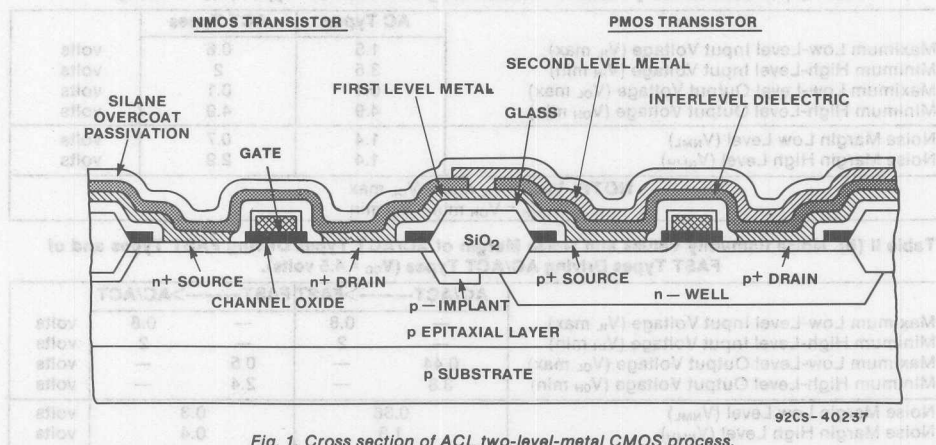


Fig. 1. Cross section of ACL two-level-metal CMOS process.

### Noise Immunity and Noise Margin

Table II shows the input noise immunity values ( $V_{IL\max}$  and  $V_{IH\min}$ ) for AC and ACT devices, the output voltage specifications, and the calculated noise margins under two conditions: (1) interfacing with like members of the same family, and (2) interfacing with bipolar FAST types. The noise margins shown in Table II (a), for AC and ACT types only, apply for the temperature range of  $-55$  to  $+125^\circ\text{C}$ . In Table II (b), the interface noise margins are limited to  $0$  to  $+70^\circ\text{C}$ , the commercial temperature range of FAST types. These tables illustrate one of the most important attributes of the CMOS AC/ACT family when compared to the FAST family; namely, designs that use the AC-series CMOS types have over three times the noise margin of the FAST family in the same design. Hence, new designs taking advantage of the higher speeds of these types should use the 1.4-volt noise margin of the AC family to gain the extra system noise margin of one volt.

### Input Current/Voltage Characteristic

The inputs of the AC/ACT devices have the dual-diode clamping circuit shown in Fig. 4. This circuit serves two important needs. (1) Ringing voltages above  $V_{CC}$  and below ground caused by the RLC interface equivalent circuit are clamped to within one diode drop of  $V_{CC}$  and ground, thereby reducing EMI. (2) Electrostatic discharge (ESD) is shunted away from the gate oxide of input transistors. Between  $-0.5$  volt and  $V_{CC}$  plus  $0.5$  volt (see Fig. 5), the input current is typically under the  $\pm 1$  nanoampere typical leakage of the biased input diodes. Beyond  $-0.5$  volt and  $V_{CC}$  plus  $0.5$  volt, the diodes are forward biased and clamping action begins. The diodes can handle large junction currents ( $\pm 400$  milliamperes for under one second). For continuous clamping action over the operating temperature range, the aluminum input metallization traces are reliably sized for  $\pm 20$  milliamperes as shown in Fig. 5. Note that it is the aluminum traces and not the diode junctions that are the limiting circuit elements.

### Input Termination

The input resistance of AC/ACT types is very high, typically  $10^9$  ohms, and the input capacitance is a few picofarads.

When unterminated inputs are left floating, they can easily pick up stray charge and move the transistor into the linear operating voltage range between  $V_{IL}$  and  $V_{IH}$ . When this transfer takes place, logic malfunction could occur, oscillation may occur, and operating current goes up. Consequently, all unused CMOS inputs must be terminated. Terminations may be directly to  $V_{CC}$  or to ground or made by means of a shunt resistor. Specification information on input termination design rules is given in the **Design Considerations** section later in this Manual.

### Input/Output ESD Protection

As mentioned, AC/ACT device inputs have a resistor-diode protection network, shown in Fig. 4, that protects the gate oxide from electrostatic discharge (ESD) damage. The network provides protection to levels greater than two kilovolts in all modes pertaining to the input, as shown in Fig. 6. This two-kilovolt figure was arrived at by the testing of devices in the ESD test circuit shown in Fig. 7 while conforming to the MIL-STD test requirements.

### Input Interaction

Another effect of the input-protection network is the imposition of a parasitic transistor between adjacent input pins. Fig. 8 shows this transistor. This parasitic transistor action may cause undesirable interaction between adjacent inputs if the input level is less than ground. In AC/ACT devices, gain of the transistor ( $\alpha = I_c / I_e$ ) is minimized to less than  $0.001$ , thereby permitting proper logic operation in the presence of large below-ground transient voltages.

### Input Capacitance

The input capacitance  $C_i$  as a function of input voltage is shown in Fig. 9 for typical AC and ACT types. Note that  $C_i$  has peak values at the respective input-voltage switch point of  $1.5$  volts for ACT and  $2.5$  volts for AC types. Capacitance on either side of the peak is a summation of package, lead-frame, reverse-biased input diode, and CMOS gate-to-source/drain capacitance. The peak capacitance results from the Miller-effect multiplication of the gate-to-drain capacitance in the high-gain linear-transition region. The value of  $C_i$  that most typically represents the average loading effect is  $7.5$  picofarads for AC and ACT inputs.

Table II (a). Noise Immunity Values and Noise Margin for AC/ACT Types ( $V_{CC} = 5$  volts).

	AC Types	ACT Types	
Maximum Low-Level Input Voltage ( $V_{IL\max}$ )	1.5	0.8	volts
Minimum High-Level Input Voltage ( $V_{IH\min}$ )	3.5	2	volts
Maximum Low-Level Output Voltage ( $V_{OL\max}$ )	0.1	0.1	volts
Minimum High-Level Output Voltage ( $V_{OH\min}$ )	4.9	4.9	volts
Noise Margin Low Level ( $V_{NML}$ )	1.4	0.7	volts
Noise Margin High Level ( $V_{NMH}$ )	1.4	2.9	volts
NOTE: $V_{NML} = V_{IL\max} - V_{OL\max}$ $V_{NMH} = V_{OH\min} - V_{IH\min}$			

Table II (b). Noise Immunity Values and Noise Margin of AC/ACT Types Driving FAST Types and of FAST Types Driving AC/ACT Types ( $V_{CC} = 4.5$  volts).

	AC/ACT	FAST	FAST	AC/ACT	
Maximum Low-Level Input Voltage ( $V_{IL\max}$ )	—	0.8	—	0.8	volts
Minimum High-Level Input Voltage ( $V_{IH\min}$ )	—	2	—	2	volts
Maximum Low-Level Output Voltage ( $V_{OL\max}$ )	0.44	—	0.5	—	volts
Minimum High-Level Output Voltage ( $V_{OH\min}$ )	3.8	—	2.4	—	volts
Noise Margin Low Level ( $V_{NML}$ )	0.36	—	0.3	—	volts
Noise Margin High Level ( $V_{NMH}$ )	1.8	—	0.4	—	volts

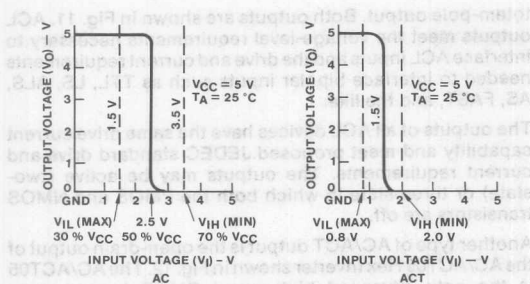


Fig. 3. ACL I/O switching characteristic for a nominal  $V_{CC}$  of 5 volts.

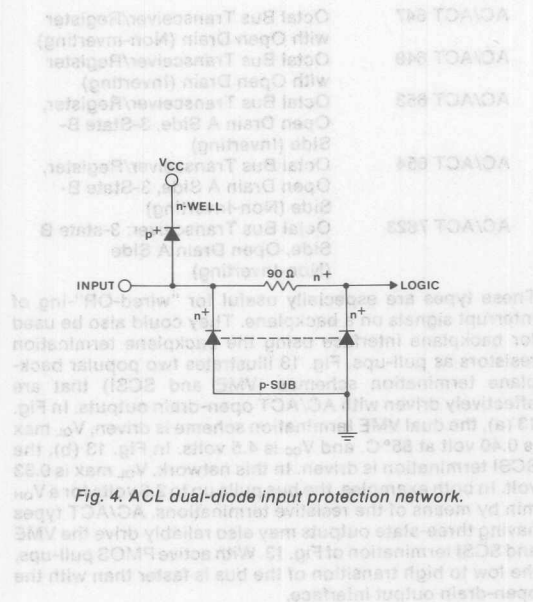


Fig. 4. ACL dual-diode input protection network.

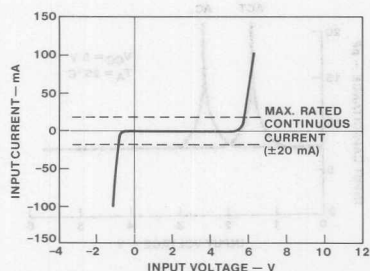


Fig. 5. ACL input characteristic.

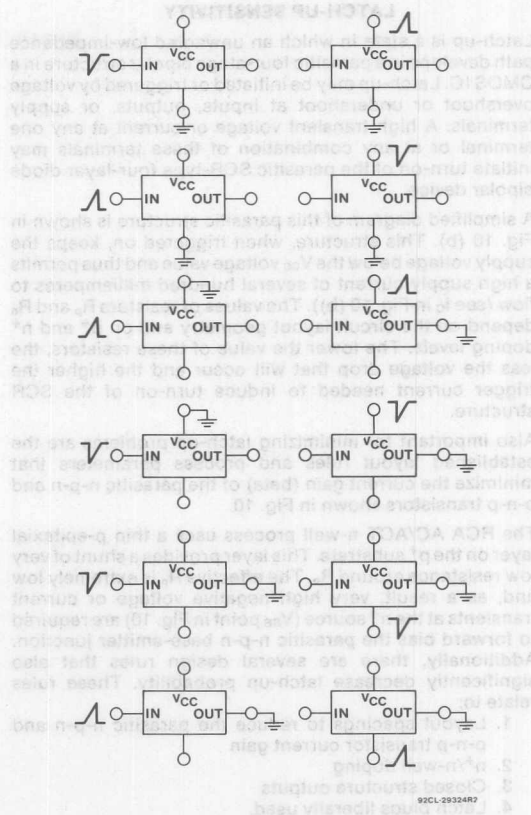


Fig. 6. Electrostatic discharge (ESD) test modes.

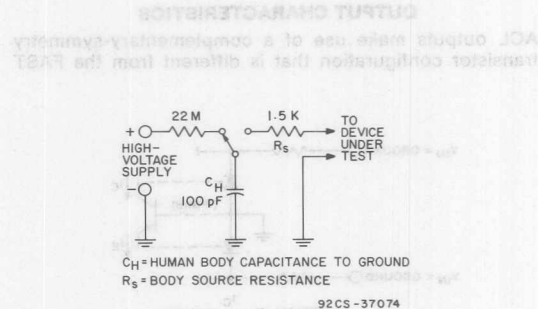


Fig. 7. Test circuit for measuring electrostatic discharge (ESD) in AC/ACT circuits. The rise time at the output terminal should be  $13 \pm 2$  ns.



## LATCH-UP SENSITIVITY

Latch-up is a state in which an unwanted low-impedance path develops in a parasitic four-stage bipolar structure in a CMOS IC. Latch-up may be initiated or triggered by voltage overshoot or undershoot at inputs, outputs, or supply terminals. A high transient voltage or current at any one terminal or at any combination of these terminals may initiate turn-on of the parasitic SCR-type four-layer diode bipolar device.

A simplified diagram of this parasitic structure is shown in Fig. 10 (b). This structure, when triggered on, keeps the supply voltage below the  $V_{CC}$  voltage value and thus permits a high supply current of several hundred milliamperes to flow (see  $I_C$  in Fig. 10 (b)). The values of resistors  $R_p$  and  $R_n$  depend on the circuit layout geometry and on  $p^+$  and  $n^+$  doping levels. The lower the value of these resistors, the less the voltage drop that will occur and the higher the trigger current needed to induce turn-on of the SCR structure.

Also important for minimizing latch-up problems are the established layout rules and process parameters that minimize the current gain ( $\beta$ ) of the parasitic n-p-n and p-n-p transistors shown in Fig. 10.

The RCA AC/ACT n-well process uses a thin p-epitaxial layer on the  $p^+$  substrate. This layer provides a shunt of very low resistance around  $R_p$ . The effective  $R_p$  is extremely low and, as a result, very high negative voltage or current transients at the  $n^+$  source ( $V_{SS}$  point in Fig. 10) are required to forward bias the parasitic n-p-n base-emitter junction. Additionally, there are several design rules that also significantly decrease latch-up probability. These rules relate to:

1. Layout spacings to reduce the parasitic n-p-n and p-n-p transistor current gain
2.  $n^+/n$ -well doping
3. Closed structure outputs
4. Latch plugs liberally used.

The current transient at any input or output terminal that could potentially trigger latch-up of AC/ACT ICs is typically more than  $\pm 400$  milliamperes at  $25^\circ\text{C}$ . Measurements are made at all terminals to assure that they have a latch current of over  $\pm 100$  milliamperes at  $125^\circ\text{C}$ . The absolute maximum dc rating in AC/ACT data sheets and in the proposed industry JEDEC Standard No. 20 is  $\pm 20$  milliamperes at inputs and  $\pm 50$  milliamperes at outputs.

## OUTPUT CHARACTERISTICS

ACL outputs make use of a complementary-symmetry transistor configuration that is different from the FAST

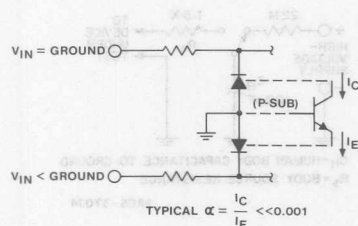


Fig. 8. Parasitic n-p-n transistor between adjacent pins imposed by input protection network.

totem-pole output. Both outputs are shown in Fig. 11. ACL outputs meet the voltage-level requirements necessary to interface ACL inputs and the drive and current requirements needed to interface bipolar inputs such as TTL, LS, ALS, AS, FAST, and the like.

The outputs of all ACL devices have the same drive current capability and meet proposed JEDEC standard drive and current requirements. The outputs may be active (two-state) or three-state in which both the PMOS and NMOS transistors are off.

Another type of AC/ACT output is the open-drain output of the AC/ACT05 Hex Inverter shown in Fig. 12. The AC/ACT05 is the only advanced high-speed CMOS inverter type having outputs that can be used for a "wired-OR" arrangement. There is, however, a very useful group of octal transceiver types having open-drain outputs. These types are listed below.

AC/ACT 647	Octal Bus Transceiver/Register with Open Drain (Non-Inverting)
AC/ACT 649	Octal Bus Transceiver/Register with Open Drain (Inverting)
AC/ACT 653	Octal Bus Transceiver/Register, Open Drain A Side, 3-State B-Side (Inverting)
AC/ACT 654	Octal Bus Transceiver/Register, Open Drain A Side, 3-State B-Side (Non-Inverting)
AC/ACT 7623	Octal Bus Transceiver; 3-state B Side, Open Drain A Side (Non-Inverting)

These types are especially useful for "wired-OR"-ing of interrupt signals on a backplane. They could also be used for backplane interface using the backplane termination resistors as pull-ups. Fig. 13 illustrates two popular backplane termination schemes (VME and SCSI) that are effectively driven with AC/ACT open-drain outputs. In Fig. 13 (a), the dual VME termination scheme is driven,  $V_{OL}$  max is 0.40 volt at  $85^\circ\text{C}$ , and  $V_{CC}$  is 4.5 volts. In Fig. 13 (b), the SCSI termination is driven. In this network,  $V_{OL}$  max is 0.33 volt. In both examples, the bus pulls up to 2.6 volts for a  $V_{OH}$  min by means of the resistive terminations. AC/ACT types having three-state outputs may also reliably drive the VME and SCSI termination of Fig. 13. With active PMOS pull-ups, the low to high transition of the bus is faster than with the open-drain output interface.

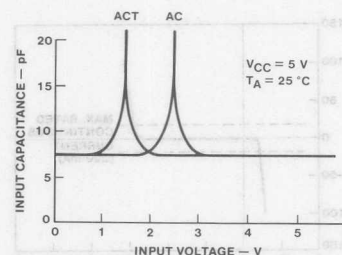
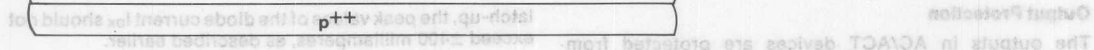


Fig. 9. Variation of input capacitance with voltage for typical AC/ACT types.



**CMOS OUTPUT** **FAST OUTPUT**

Fig. 11. AC/ACT output, a complementary-symmetry transistor configuration, compared with FAST output, a totem-pole configuration.

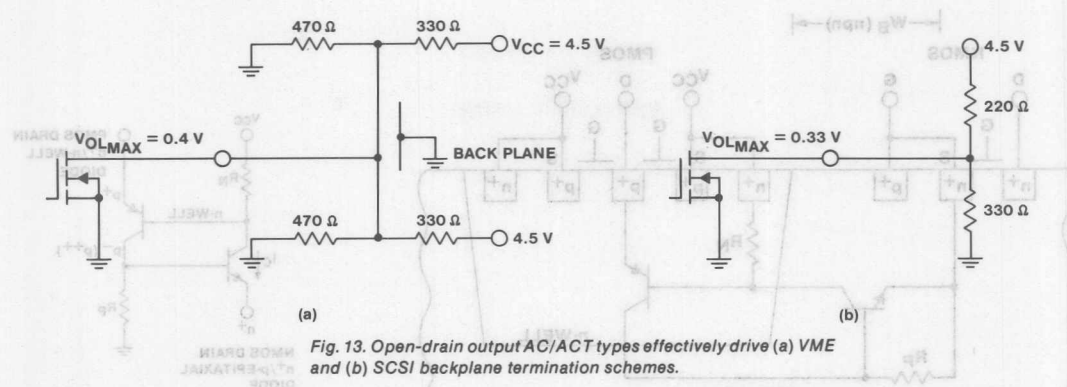


Fig. 13. Open-drain output AC/ACT types effectively drive (a) VME and (b) SCSI backplane termination schemes.

### Output Protection

The outputs in AC/ACT devices are protected from electrostatic discharge (ESD) damage by an integral inherent diode structure. Fig. 14 shows these diodes. These protective diodes are effective because of the large geometries (widths) of the output transistors. The diodes are comprised of the drain and the n-substrate junction of the p device and of the drain and the p-well junction of the n-device. This network provides protection to voltage levels greater than two kilovolts in all electrostatic discharge modes pertaining to the output (for these modes, see Fig. 6).

### Output Current

AC/ACT outputs are specified for both CMOS and bipolar FAST loads. CMOS inputs are voltage sensitive and the only current is leakage current. The output voltage test for CMOS interfacing is specified for  $I_O$  at  $\pm 50$  microamperes (50 CMOS loads). The outputs are also specified for  $I_O$  at  $\pm 24$  milliamperes (15 FAST loads). The corresponding  $V_{OL}$  max and  $V_{OH}$  min for the outputs are given in Table III.

Note that for the AC-series types, operation down to 1.5 volts is specified. Output current is specified at 1.5 volts and also at 3 volts. This worst-case 3-volt rating is increasingly important because it corresponds to the new low-voltage logic standard (JEDEC Std. No. 8) of  $3.3 \pm 0.3$  volts. As CMOS technology shrinks to under one micron, reliability, operating power, and, most of all, switching noise all point toward more favorable results with a supply voltage of 3.3 volts than with 5-volt ones. At 3.3 volts, AC/ACT types consume only 40 per cent of the operating power of 5-volt operation, and switching speed is decreased by an average of only 60 per cent. Also, as will be covered in the section on **Design Considerations**, TTL interface is realizable at  $3.3 \pm 0.3$  volts.

The maximum current per output pin ( $I_O$ ) is  $\pm 50$  milliamperes. This maximum current rating is specified when the outputs ( $V_O$ ) are in their active regions, that is, greater than -0.5 volt but less than  $V_{CC}$  plus 0.5 volt. The maximum current rating per power pin,  $V_{CC}$  or ground, is  $\pm 100$  milliamperes for up to four outputs; for each additional output the rating is increased by  $\pm 25$  milliamperes. When the output voltage exceeds  $V_{CC}$  by more than 500 millivolts or is below ground by more than 500 millivolts, the output protection diodes turn on and conduct current. To avoid

latch-up, the peak values of the diode current  $I_{OK}$  should not exceed  $\pm 400$  milliamperes, as described earlier.

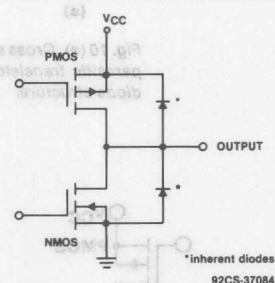


Fig. 14. Inherent diode structure that protects AC/ACT outputs from electrostatic discharge damage to levels greater than two kilovolts.

### Output-Current Interfacing Capability

A comparison of the output drive capabilities of AC/ACT types with those of FAST types is as follows.

FAST capability is expressed in unit loads (ULs) where the load is specified to be an input of the same family. This specification assures that the worst-case low- and high-input thresholds will be met and the existing margins of noise immunity preserved.

AC/ACT capability is expressed as source/sink current at a specified output voltage. Because AC/ACT types require virtually no input current, the unit-load concept does not apply.

With a specified output sink current drive of 24 milliamperes at 0.44 volt (at 85°C), each AC/ACT output can drive 24,000 AC/ACT inputs. With a 50-microampere/0.1-volt specification, each AC/ACT output can drive 480 AC/ACT inputs. Each AC/ACT output has a drive capability of 15 FAST loads and maintains a  $V_{OL}$  under 0.5 volt over the full temperature range.

The standardized RCA and the proposed JEDEC output characteristics are shown in Table III.

**Table III. Standard RCA and Proposed JEDEC Output Characteristics**  
**AC Series (•For ACT Series, Specifications Only @  $V_{CC} = 4.5$  V and 5.5 V Apply)**

CHARACTERISTIC		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125 (74) -55 to +125 (54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		Min.	Max.	Min.	Max.	Min.	Max.	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # •	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			• -0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			• -24	4.5	3.94	—	3.8	—	3.7	—	
			• -75	5.5	—	—	3.85	—	—	—	
			• -50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # •	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			• 0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			• 24	4.5	—	0.36	—	0.44	—	0.5	
			• 75	5.5	—	—	—	1.65	—	—	
			• 50	5.5	—	—	—	—	—	1.65	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series. 75 ohms for 54AC/ACT Series.

NOTE: Specifications at 1.5 volts are not part of the JEDEC proposal.

### Output Curves

In Figs. 15 and 16 the standardized family output characteristic plots are provided. Both typical and worst-case (min) curves plot the  $I_{OL}$  (sink) and  $I_{OH}$  (source) current as a function of drain-to-source output transistor voltage drop ( $V_{DS}$ ). The line at 50 milliamperes is the boundary between safe, continuous operating regions of current drain and areas where only transients are permitted.

### Output Short-Circuit Current (Backdriving)

Note that in Fig. 15 short-circuit currents of  $\pm 200$  milliamperes are typical for AC/ACT outputs at a  $V_{CC}$  of five volts. Backdriving these outputs during PC board test by forcing outputs to ground, for example, is permissible with the limitations that only one output per IC be backdriven at any one time and for only one second maximum. For durations longer than one second, the IC may become too hot. Fortunately, because the epitaxial-based process is essentially latch free, no danger of latch-up results from backdriving.

### Output Simultaneous Switching Transients

From Fig. 15, it is evident that very large switching transients can be absorbed by AC/ACT output transistors. Fig. 17 illustrates how large transient currents are typically generated for the charge or discharge of an AC/ACT output using a 50-picofarad load and a  $V_{CC}$  of five volts. The discharge time through the n-device of the output transistor is typically three nanoseconds, even though the capacitor discharge current is typically 83 milliamperes, as shown in the following calculation.

$$I_C = C (dv/dt) = 50 \text{ pF} (5 \text{ V}/3 \text{ ns}) = 83 \text{ mA}$$

The ON resistance of the p and n channels is typically 10 ohms each during peak switching transient periods. Thus, it

is possible that switching currents of  $\pm 200$  milliamperes per output may occur. For octal types, where bytes are simultaneously switched at common edges, the total peak switching current could approach  $8 \times 200$  milliamperes or 1.6 amperes. In practice, however, the actual current is lower because it spreads somewhat as a result of the deviations in peak switching times. These currents cause device  $V_{CC}$  and ground bus voltage drops that vary with each output and hence cause different output delays. These delays spread the switching current over one to two nanoseconds.

Fig. 18 shows that four inductances contribute to the on-chip ground potential  $V_G$ . These inductances are L1, the effective on-chip ground path inductance; L2, the chip bond-pad/wire/lead-frame inductance; L3, the IC lead inductance; and, L4, the printed-circuit board inductance path to earth or reference ground. Fig. 19 illustrates the lifting of ground as a result of the inductances L1 through L4 when an AC/ACT device switches. Instantaneously, the chip sees  $V_G$  as ground and causes the following IC performance effects.

1. If n outputs switch and one output is a steady-state low, the  $V_G$  will reflect on to the unswitched output as the peak low-level output voltage  $V_{OLP}$ , as shown in Fig. 20 (b) for an eight-output device.
2. The instantaneous gate-to-source voltage decreases by a magnitude of  $V_G$  volts. This decrease reduces the transistor  $g_m$ , raises the  $R_{ON}$ , and increases the transition time of the output stage and the delay time.
3. Input noise immunity is instantaneously decreased by  $V_G$  volts and, as a result, internally stored data in latches or flip-flops could be upset.



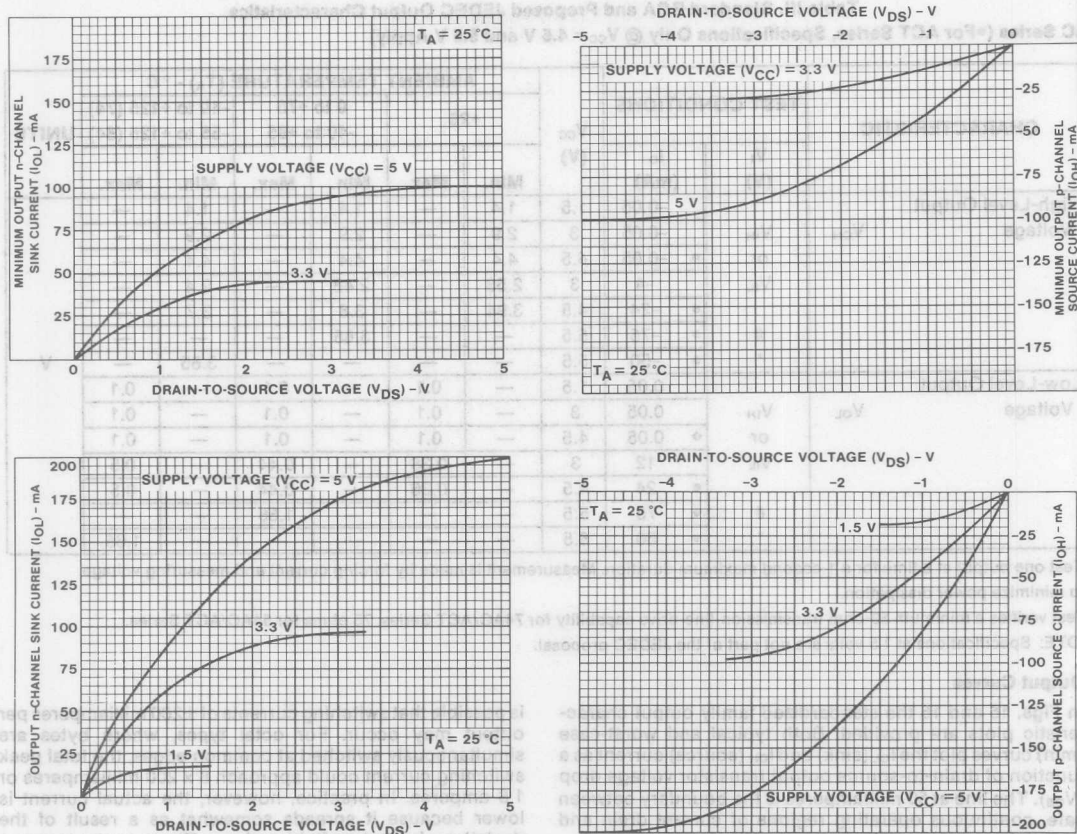


Fig. 15. Minimum and typical output characteristics at  $+25^\circ\text{C}$  for AC/ACT advanced high-speed CMOS types.

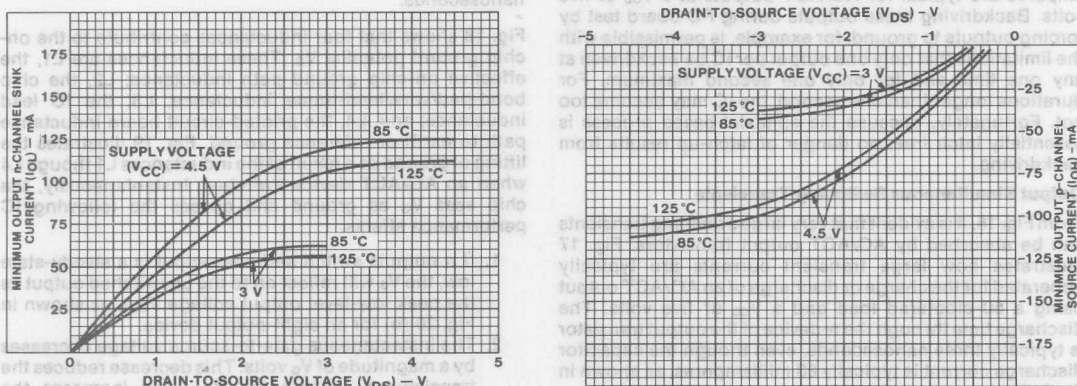


Fig. 16. Minimum output characteristic curves at  $+85^\circ\text{C}$  and  $+125^\circ\text{C}$  for AC/ACT advanced high-speed CMOS types.



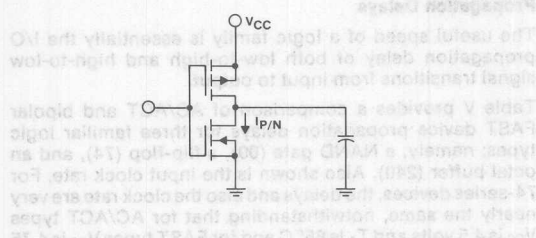


Fig. 17. Generation of large transient currents for charge or discharge of an AC/ACT output. Load = 50 picofarads;  $V_{CC}$  = 5 volts.

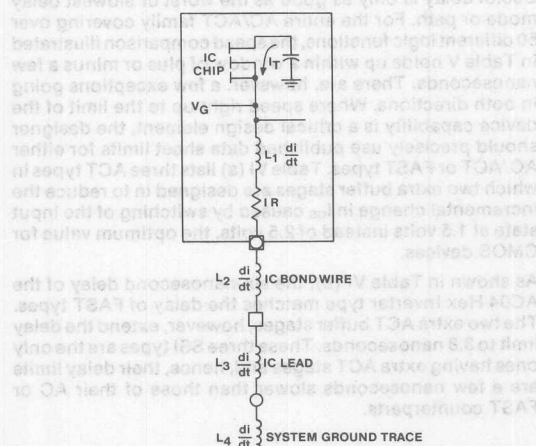


Fig. 18. IC ground path and four contributing inductances.

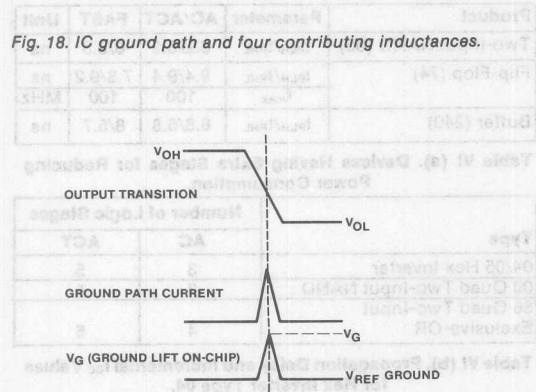


Fig. 19. Ground lift caused by switching current transients through inductances described in Fig. 18.

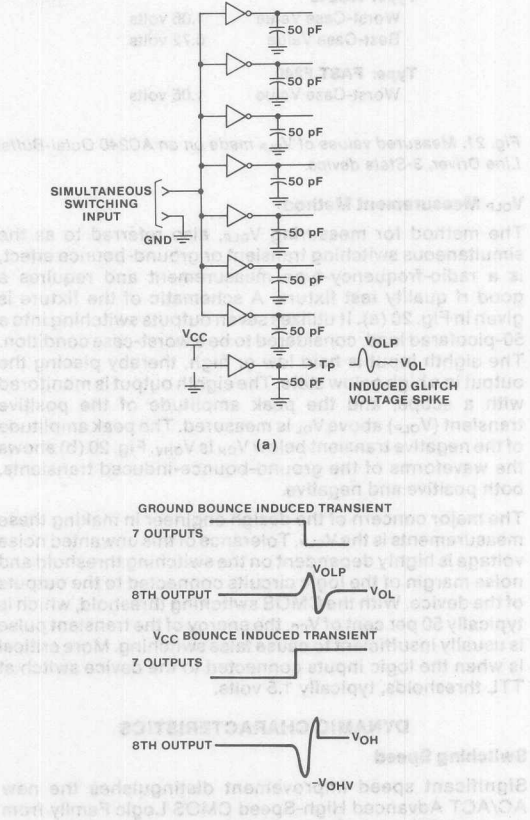


Fig. 20. Test circuit (a) and waveform (b) of simultaneous switching transient.

### Sample Measurement of $V_{OLP}$

Fig. 21 shows actual sample measurement values of the peak low-level output voltage  $V_{OLP}$  measured on an AC240, an Octal-Buffer Line Driver, 3-State device. The worst-case  $V_{OLP}$ , 1.06 volts, occurs at pin 18, which is furthest from pin 10 ground. The best case  $V_{OLP}$ , 0.720 volt occurs at pin 9, closest to pin 10. This performance is very reasonable for a buffer having a typical delay of 3.5 nanoseconds. RCA advanced high-speed CMOS octal logic devices have been designed to minimize the effective on-chip  $L_1$  (Fig. 18) and also to minimize  $L_2$ , the effective chip-to-lead-frame inductance.  $L_3$  is the inductance of a "corner-pin" dual-in-line (DIP) or small outline (SOP) package, and  $L_4$  is the inductance of the fixture ground-return path. This last value is very small (see next section on **Measurement Method**). For comparison, a bipolar FAST F240 type was identically measured. Its  $V_{OLP}$  is nearly identical, the worst-case value being 1.05 volts.

<b>Type: AC240</b>		
Worst-Case Value	1.06 volts	
Best-Case Value	0.72 volts	
<b>Type: FAST F240</b>		
Worst-Case Value	1.05 volts	

Fig. 21. Measured values of  $V_{OLP}$  made on an AC240 Octal-Buffer Line Driver, 3-State device.

#### $V_{OLP}$ Measurement Method

The method for measuring  $V_{OLP}$ , also referred to as the simultaneous switching transient or ground-bounce effect, is a radio-frequency-type measurement and requires a good rf quality test fixture. A schematic of the fixture is given in Fig. 20 (a). It utilizes seven outputs switching into a 50-picofarad load, considered to be a worst-case condition. The eighth input is held low or high, thereby placing the output in a high or low state. The eighth output is monitored with a scope, and the peak amplitude of the positive transient ( $V_{OLP}$ ) above  $V_{OL}$  is measured. The peak amplitude of the negative transient below  $V_{OH}$  is  $V_{OHV}$ . Fig. 20 (b) shows the waveforms of the ground-bounce-induced transients, both positive and negative.

The major concern of the design engineer in making these measurements is the  $V_{OLP}$ . Tolerance of this unwanted noise voltage is highly dependent on the switching threshold and noise margin of the logic circuits connected to the outputs of the device. With the CMOS switching threshold, which is typically 50 per cent of  $V_{CC}$ , the energy of the transient pulse is usually insufficient to cause false switching. More critical is when the logic inputs connected to the device switch at TTL thresholds, typically 1.5 volts.

### DYNAMIC CHARACTERISTICS

#### Switching Speed

Significant speed improvement distinguishes the new AC/ACT Advanced High-Speed CMOS Logic Family from the HC/HCT High-Speed CMOS Logic Family. Table IV places each CMOS logic family with the speed-equivalent TTL family. From the standpoint of speed, the AC/ACT family substitutes very adequately for the TTL FAST, ALS, AS, and S families. It is not recommended, however, to directly substitute FAST, AS, S, or AC/ACT for HC/HCT or LSTTL logic because of the three times faster switching edges of the former group compared to the latter. As will be covered in the **Design Considerations** section, these faster families require transmission-line interconnect considerations, terminations, superior decoupling, and careful PC board layout to keep switching noise generation under control.

Table IV. Guide for Substituting CMOS Logic Family Types for TTL Families.

CMOS Logic Family	TTL Family					
	TTL	LSTTL	ALS	S	FAST	AS
HC/HCT	X	X	X <sup>#</sup>			
AC/ACT	*	*	X*	X	X	X

<sup>#</sup>HC/HCT substitutes when ALS is used versus LS for lower power.

AC/ACT substitutes when ALS is used versus LS for higher speed.

\*There is too large a difference in speed and noise/EMI generation for AC/ACT to reliably substitute for TTL, LSTTL, or HC/HCT.

#### Propagation Delays

The useful speed of a logic family is essentially the I/O propagation delay of both low-to-high and high-to-low signal transitions from input to output.

Table V provides a comparison of AC/ACT and bipolar FAST device propagation delays for three familiar logic types; namely, a NAND gate (00), a flip-flop (74), and an octal buffer (240). Also shown is the input clock rate. For 74-series devices, the delays and also the clock rate are very nearly the same, notwithstanding that for AC/ACT types  $V_{CC}$  is 4.5 volts and  $T_A$  is 85°C and for FAST types  $V_{CC}$  is 4.75 volts and  $T_A$  is 70°C. These test conditions are clearly in favor of FAST by about five per cent. Also evident from the data sheet extractions in Table V are the balanced delay of AC/ACT types and the unbalanced ( $t_{PLH}$  versus  $t_{PHL}$ ) delay of the bipolar types.

Useful delay is only as good as the worst or slowest delay mode or path. For the entire AC/ACT family covering over 50 different logic functions, the speed comparison illustrated in Table V holds up within a window of plus or minus a few nanoseconds. There are, however, a few exceptions going in both directions. Where speed right up to the limit of the device capability is a critical design element, the designer should precisely use published data sheet limits for either AC/ACT or FAST types. Table VI (a) lists three ACT types in which two extra buffer stages are designed in to reduce the incremental change in  $I_{CC}$  caused by switching of the input state at 1.5 volts instead of 2.5 volts, the optimum value for CMOS devices.

As shown in Table VI (b), the six-nanosecond delay of the AC04 Hex Inverter type matches the delay of FAST types. The two extra ACT buffer stages, however, extend the delay limit to 8.8 nanoseconds. These three SSI types are the only ones having extra ACT stages and, hence, their delay limits are a few nanoseconds slower than those of their AC or FAST counterparts.

Table V. Comparison of Switching Speed for Three 74-Series AC/ACT and FAST Logic Functions.

Product	Parameter	AC/ACT	FAST	Unit
Two-Input NAND (00)	$t_{PLH}/t_{PHL}$	6.2/6.2	6/5.3	ns
Flip-Flop (74)	$t_{PLH}/t_{PHL}$	9.4/9.4	7.8/9.2	ns
	$f_{max}$	100	100	MHz
Buffer (240)	$t_{PLH}/t_{PHL}$	6.8/6.8	8/5.7	ns

Table VI (a). Devices Having Extra Stages for Reducing Power Consumption.

Type	Number of Logic Stages	
	AC	ACT
04/05 Hex Inverter	3	5
00 Quad Two-Input NAND	3	5
86 Quad Two-Input Exclusive-OR	4	5

Table VI (b). Propagation Delay and Incremental  $I_{CC}$  Values for Hex Inverter Type 04.

Parameter	AC	ACT	FAST	Unit
$t_{PLH}/t_{PHL}$	6/6	8.8/8.8	6/5.3	ns
$\Delta I_{CC}$ per Input	—	0.5*	—	mA

\*For three stages instead of five this value would be about three milliamperes per input.

### Propagation Delay Performance Curves

Fig. 22 shows the typical normalized propagation delay as a function of capacitance loading at supply voltages of 1.5, 3.3, and 5 volts. The reference load is 50 picofarads, the rated value given in the device data sheet. Fig. 23 shows the typical normalized propagation delay as a function of supply voltage. This curve shows that AC-Series types are typically 30 per cent slower at 3.3 volts than at the referenced 5 volts. At a supply voltage of 1.5 volts, the speed is four times slower compared to 5 volts but still is quite fast. In Fig. 24, the normalized AC/ACT propagation delay variation with chip operating ambient temperature is given for operation at 1.5, 3.3, and 5 volts. From the 5-volt curve, it can be concluded that AC/ACT types slow down by 0.3 per cent per °C, a useful number to have available for reference.

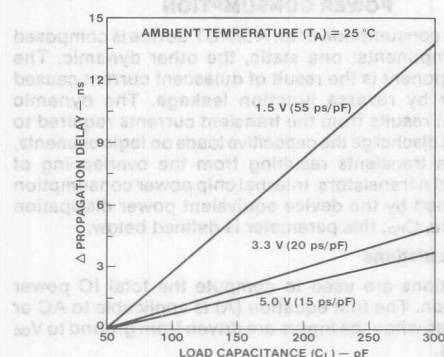


Fig. 22. Typical change in propagation delay as a function of load capacitance for AC/ACT types.

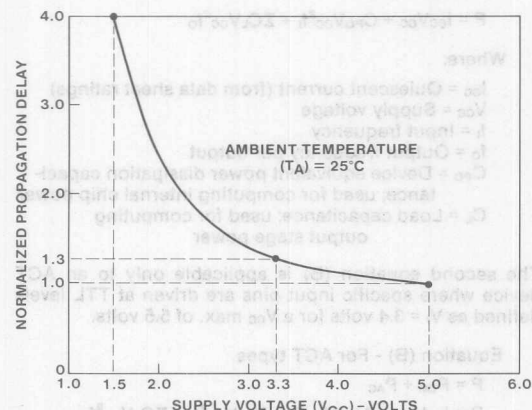


Fig. 23. Normalized propagation delay as a function of supply voltage for AC types.

### Output Edge Rates/Transition Times

The typical propagation delay of an AC/ACT gate or buffer is 3.5 nanoseconds (at  $V_{CC} = 5$  volts,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50$  picofarads), and the high speed of all AC/ACT types necessitate quick and predictable output transition times. Typical AC/ACT output transition times are shown in Table VII. If speed is needed, certainly the output transition time is an important factor; but it is gained at the cost of a high-

spectral-content output. Also, depending on output inductance values, the outputs may have ringing problems.

Fortunately, unlike bipolar FAST logic, the design engineer may insert series resistors ( $R_S$ ) in the output circuit, as shown in Fig. 25, to reduce the spectral content, dampen ringing, and act as a series terminator. Propagation delay, however, will increase as a result of the series resistor and the associated total shunt capacitance  $C_S$ . For CMOS loads, an  $R_S$ , even up to several kilohms in value, will not affect input switching because the input resistance ( $R_i$ ) is greater than 1000 megohms. For bipolar FAST devices, however, adding a series resistor results in increased values of  $V_{IL}$  because  $I_{IL}$  is 1.6 milliamperes. Hence, 100 ohms is probably the maximum value for  $R_S$  with FAST ICs. This topic is covered in more detail in the **Design Considerations** section of this Manual.

Table VII. Typical Output Transition Time ( $t_{TLH}$ ,  $t_{THL}$ ). Measured Between the 10 and 90 Per Cent Transition Points. The ambient temperature is  $25^\circ\text{C}$

$C_L$ (pF)	$V_{CC}$ (volts)	Typical $t_{THL}$ , $t_{TLH}$ (nanoseconds)
50	1.5	8
50	3.3	3
50	5	2.5
150	1.5	20
150	3.3	8
150	5	6
300	1.5	35
300	3.3	11
300	5	10

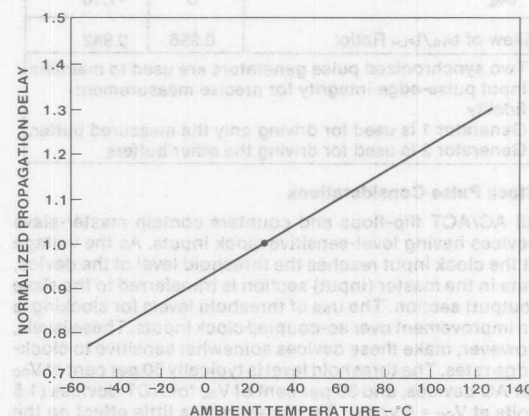


Fig. 24. Normalized propagation delay as a function of ambient temperature for AC/ACT types.

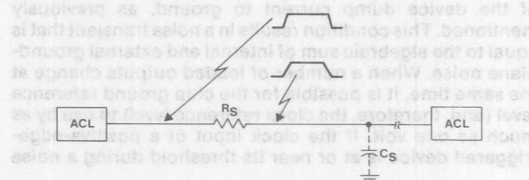


Fig. 25. Use of series termination resistor to increase output edge rates.

### Incremental Propagation Delay Caused by Simultaneous Switching

Table VIII illustrates the effects of ground and  $V_{CC}$  "bounce" resulting from the simultaneous switching of eight Octal-Buffer outputs. Note that the incremental delay added to  $t_{PHL}$  is less than that added to  $t_{PLH}$ . The reason for this difference is that the RCA chip design and the design of the bond-pad-to-lead frame are geared heavily to reducing the very critical ground loop inductance because of the 0.8-volt  $V_{IL}$  of ACT and FAST inputs. On the high side, where  $V_{IH}$  is two volts and the loaded  $V_{OH}$  is 3.8 volts, the  $V_{CC}$  bounce is not so critical. Also shown in Table VIII is the shift in skew due to  $V_{CC}$  and ground-bounce effects. The cause of these effects is described earlier in this Manual starting under the heading **Output Simultaneous Switching Transients**.

**Table VIII. Incremental Propagation Delay of an AC244 Octal Non-Inverting Buffer Type.**

Conditions:  $V_{CC} = 5$  volts;  $C_L = 50$  picofarads;  $T_A = 25^\circ\text{C}$ .

	Number of Outputs Switching	
	1 (Best)	8 (Worst)
Buffer Measured:		
Input Pin	2	2*
Output Pin	18	18
Data (ns):		
$t_{PLH}$	4.9	6.41
$t_{PHL}$	4.88	6.04
Incremental Delay (ns) Referred To One Buffer Switching:		
$t_{PLH}$	0	+1.51
$t_{PHL}$	0	+1.16
Skew of $t_{PHL}/t_{PLH}$ Ratio:	0.996	0.942
*Two synchronized pulse generators are used to maintain input pulse-edge integrity for precise measurement fidelity. Generator 1 is used for driving only the measured buffer. Generator 2 is used for driving the other buffers.		

### Clock Pulse Considerations

All AC/ACT flip-flops and counters contain master-slave devices having level-sensitive clock inputs. As the voltage at the clock input reaches the threshold level of the device, data in the master (input) section is transferred to the slave (output) section. The use of threshold levels for clocking is an improvement over ac-coupled clock inputs. These levels, however, make these devices somewhat sensitive to clock-edge rates. The threshold level is typically 50 per cent of  $V_{CC}$  for AC devices, and 30 per cent of  $V_{CC}$  for ACT devices (1.5 volts at  $V_{CC} = 5$  volts). Temperature has little effect on the clock threshold levels.

When clocking occurs, the internal gates and output circuits of the device dump current to ground, as previously mentioned. This condition results in a noise transient that is equal to the algebraic sum of internal and external ground-plane noise. When a number of loaded outputs change at the same time, it is possible for the chip ground reference level (and, therefore, the clock reference level) to rise by as much as one volt. If the clock input of a positive-edge-triggered device is at or near its threshold during a noise

transient period, multiple triggering can occur. To prevent this condition, the rise and fall slew rates of the clock inputs should be limited to the maximum ratings specified on the data sheet for the AC/ACT type. The AC/ACT 14 Hex Schmitt Trigger type is recommended for sharpening up slow transitions.

Maximum permissible input-clock frequency ratings on the data sheet for each clocked device require an input clock having a 50 per cent duty cycle. At these rated frequencies, the outputs will swing rail to rail, assuming no dc load on the outputs. This feature provides a very conservative and highly reliable method of rating clock-input-frequency limits that, for AC/ACT devices, equal or exceed the ratings for FAST types.

### POWER CONSUMPTION

The power consumption of an AC/ACT device is composed of two components: one static, the other dynamic. The static component is the result of quiescent current caused principally by reverse junction leakage. The dynamic component results from the transient currents required to charge and discharge the capacitive loads on logic elements, that is, the transients resulting from the overlapping of active p and n transistors. Internal chip power consumption is determined by the device equivalent power dissipation capacitance,  $C_{PD}$ ; this parameter is defined below.

#### Power Calculations

Two equations are used to compute the total IC power consumption. The first equation (A) is applicable to AC or ACT devices when the inputs are driven from ground to  $V_{CC}$  (rail to rail).

Equation (A) - For AC types

$$P = P_{DC} + P_{AC}$$

$$P = I_{CC}V_{CC} + C_{PD}V_{CC}^2f_i + \Sigma C_L V_{CC}^2f_o$$

Where:

$I_{CC}$  = Quiescent current (from data sheet ratings)

$V_{CC}$  = Supply voltage

$f_i$  = Input frequency

$f_o$  = Output frequency per output

$C_{PD}$  = Device equivalent power dissipation capacitance; used for computing internal chip power

$C_L$  = Load capacitance; used for computing output stage power

The second equation (B) is applicable only to an ACT device where specific input pins are driven at TTL levels defined as  $V_I = 3.4$  volts for a  $V_{CC}$  max. of 5.5 volts.

Equation (B) - For ACT types

$$P = P_{DC} + P_{AC}$$

$$P = I_{CC}V_{CC} + \Delta I_{CC}V_{CC}D + C_{PD}V_{CC}^2f_i + \Sigma C_L V_{CC}^2f_o$$

Where:

$\Delta I_{CC}$  = Added direct current when  $V_I = V_{CC} - 2.1$  V (TTL input high level)

$D$  = Duty cycle of clock (per cent of time high)

The temperature-dependent ratings for  $I_{CC}$  are given in Tables IX and X.



Table IX. Temperature-Dependent Rating Limits

	$V_i$ (V)	$V_{CC}$ (V)	25°C		-40 to +85°C	-55 to +125°C
			Typ. (mA)	Max. (mA)	Max. (mA)	Max. (mA)
$(\Delta I_{CC})^*$	$V_{CC} - 2.1$	4.5 to 5.5	0.2	2.4	2.8	3

\*Additional quiescent supply current per input pin, TTL inputs high, 1 unit load  
ACT load table by type shown on each data sheet.

Example: Type: ACT191; input: clock; unit load: 0.85  
 $\Delta I_{CC} = 0.85(2.4 \text{ mA}) = 2.04 \text{ mA max at } 25^\circ\text{C}$

 Table X. Maximum Quiescent Current at  $V_{CC} = 5$  volts for AC/ACT and FAST Types.

Device Complexity	AC/ACT Limit			FAST
	25°C	85°C	125°C	125°C
SSI/FF	4 $\mu\text{A}$	40 $\mu\text{A}$	80 $\mu\text{A}$	15 mA
MSI	8 $\mu\text{A}$	80 $\mu\text{A}$	160 $\mu\text{A}$	100 mA

The dynamic power due to outputs is the sum of the ac power at each output. The user must independently determine the  $C_L$  and the average frequency of each output. The latter requires estimating the average frequency of data nodes in a logic system. For example, for AC/ACT counter types, each output is inherently operating at different frequencies.

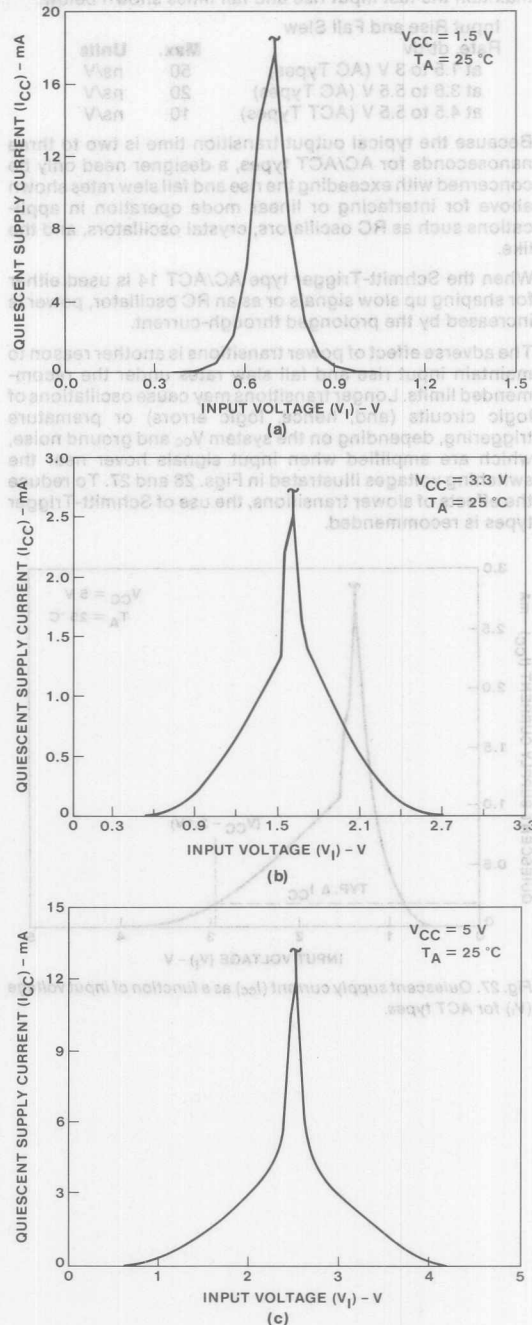
The  $C_{PD}$  or device equivalent-power-dissipation capacitance is determined by two sources of internal device power consumption:

1. Power consumed by charge and discharge of the internal device capacitance.
2. Power consumed through current switching transients.

Fig. 26 illustrates the typical  $I_{CC}$  as a function of  $V_i$  for AC devices. Note in Fig. 26 (c) that when  $V_{IN}$  equals 0 to 0.5 volt or 4.5 to 5 volts, zero current flows. Thus, no  $\Delta I_{CC}$  component is required for computing the power consumption of AC device types. The transient switching currents of an IC, however, consume power and are part of the  $C_{PD}$  value. The plots of  $I_{CC}$  and  $V_i$  of Fig. 26 show peak  $I_{CC}$  of up to 12 milliamperes. For a few nanoseconds, however, up to 100 milliamperes could flow if the plotter resolution permitted. Note that the switching points (peak current points) in the AC devices occur at approximately 50 per cent of  $V_{CC}$ . For the ACT devices (shown in Fig. 27) the switching point is at approximately 30 per cent of  $V_{CC}$ .

Fig. 27 illustrates the typical  $I_{CC}$  as a function of  $V_i$  for ACT devices. Again, if the input voltage is other than 0 to 0.5 volt or 4.5 to 5.5 volts, no  $\Delta I_{CC}$  value exists. If  $V_i$ , however, is a TTL logic high level of 2.9 volts with a  $V_{CC}$  of 5 volts, then significant  $\Delta I_{CC}$  does exist (0.2 milliamperes) and is indicated in equation (B) as the  $\Delta I_{CC}$  component.

Because the special input design of RCA ACT types reduces the value of  $\Delta I_{CC}$ , the added power is small and is usually minimal compared to FAST power. If this special input circuitry were not used, the  $\Delta I_{CC}$  values would be much higher.


 Fig. 26. Quiescent supply current ( $I_{CC}$ ) as a function of input voltage ( $V_i$ ) for AC types.



Because appreciable current flows during device input switching, as shown in Figs. 26 and 27, it is important to maintain the fast input rise and fall times shown below.

Input Rise and Fall Slew Rate, dt/dv	Max.	Units
at 1.5 to 3 V (AC Types)	50	ns/V
at 3.6 to 5.5 V (AC Types)	20	ns/V
at 4.5 to 5.5 V (ACT Types)	10	ns/V

Because the typical output transition time is two to three nanoseconds for AC/ACT types, a designer need only be concerned with exceeding the rise and fall slew rates shown above for interfacing or linear mode operation in applications such as RC oscillators, crystal oscillators, and the like.

When the Schmitt-Trigger type AC/ACT 14 is used either for shaping up slow signals or as an RC oscillator, power is increased by the prolonged through-current.

The adverse effect of power transitions is another reason to maintain input rise and fall slew rates under the recommended limits. Longer transitions may cause oscillations of logic circuits (and, hence, logic errors) or premature triggering, depending on the system  $V_{CC}$  and ground noise, which are amplified when input signals hover near the switching voltages illustrated in Figs. 26 and 27. To reduce the effects of slower transitions, the use of Schmitt-Trigger types is recommended.

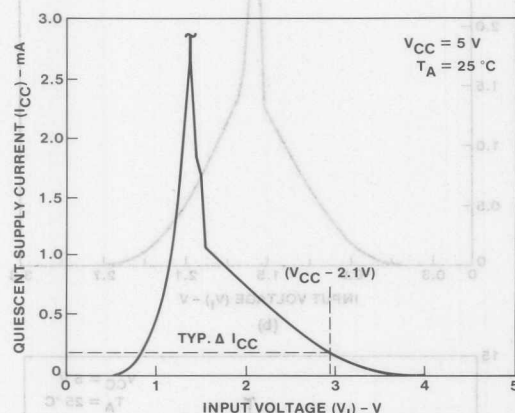


Fig. 27. Quiescent supply current ( $I_{CC}$ ) as a function of input voltage ( $V_i$ ) for ACT types.

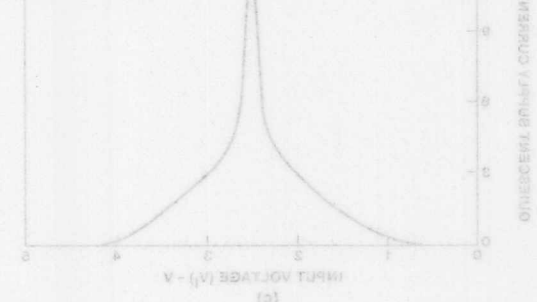


Fig. 28. Quiescent supply current ( $I_{CC}$ ) as a function of input voltage ( $V_i$ ) for AC types.

## Power Consumption of FAST and AC/ACT Types Compared

As the equations for operating power indicate, CMOS power is directly proportional to switching frequency. At standby, AC/ACT power is negligible compared to bipolar FAST power. In Table XI, one of the most widely used MSI counters (the 191 4-Bit Binary Counter) is used to illustrate that even at a continuous ten-megahertz switching rate, AC/ACT power is a fraction of the power of FAST types. By way of illustration, consider an application employing 25 such types. At an overall average switching rate of ten megahertz, with FAST types the power is 7.7 watts. With AC/ACT types, the power is only 1.4 watts for AC types and 2.6 watts for ACT types.

Table XI. Average Operating Power Comparison for FAST and AC/ACT Type 191, a 4-Bit Up/Down Binary Counter.  $V_{CC} = 5.5 \text{ V}$ ;  $T_A = 70^\circ \text{C}$ .

Family	Notes	Switching Rate			Units
		0 MHz	1 MHz	10 MHz	
AC	1	0.44	5.5	55	mW
ACT	2	49.4	59.9	104	mW
FAST	3	204	224	306	mW

Notes:

$$1. P = P_{DC} + P_{AC}$$

Where:  $P_{DC} = 5.5 \times 80 \mu\text{A}$

$$\text{and } P_{AC} = 133 \text{ pF}(5.5)^2 f_i + 50 \text{ pF}(5.5)^2 \left( \frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{16} \right) f_o \text{ (Eq. A)}$$

$$2. P = P_{DC} + P_{AC}$$

Where:  $P_{DC} = 5.5 \times 80 \mu\text{A} + 8 \times 2.8 \text{ mA} \times 0.8 \times \frac{1}{2} \times 5.5 \text{ (Eq. B)}$   
 and  $P_{AC} = 133 \text{ pF}(5.5)^2 f_i + 50 \text{ pF}(5.5)^2 \left( \frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{16} \right) f_o \text{ (Eq. A)}$

$$3. P = 5.5 \times 55 \text{ mA (0 Hz)}$$

$$P = 5.5 \times 55 \text{ mA} \times 1.1 \text{ (1 MHz)}$$

$$P = 5.5 \times 55 \text{ mA} \times 1.5 \text{ (10 MHz)}$$

## REFERENCES

JEDEC Standard No. 8, "Standard for Reduced Operating Voltages and Interface Levels for Integrated Circuits."

JEDEC Standard No. 20, "Standard For Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High Speed CMOS Devices." (In preparation).

# INTERCONNECTION OF ACL LOGIC DEVICES

Interconnections of ACL high-speed logic devices by means of single wires, coaxial cable, stripline, ribbon cable, or twisted pair must necessarily be designed to preserve the pulse waveform. Fig. 28 illustrates the basic interconnect environment and shows the pulse waveforms for both the ideal case and the practical or actual case with ACL devices. The ideal case, shown in the waveform of Fig. 28 (b) when one ACL output port is connected to an input port of another ACL port, is realizable for short interconnect lengths (less than five inches) or for the case when the line is matched by the addition of a shunt termination resistance ( $R_T$ ) in parallel with the input resistance ( $R_i$ ), as shown in Fig. 29.

If the only concern were the fidelity of the pulse waveform at the IC input or load end of the interconnection, which is often but not always the case, then a series termination scheme can be used, as shown in Fig. 29 (a). The termination resistor  $R_T$  is selected to make  $R_T$  plus  $R_i$  equal to  $Z_0$ . If the output resistance  $R_o$  is 25 ohms and the characteristic impedance  $Z_0$  is 100 ohms, then  $R_T$  is 75 ohms. This approach is called ideal series matching.

By studying the interconnect environment, the designer quickly learns that the interconnection distance is "short," there is no concern and the waveform of Fig. 28 (b) can prevail fairly well. The major design question, however, is what is "short"? Basic interconnect theory, as covered in the references given at the end of this section, states that transmission-line effects or wave effects become an important design consideration when the length of the interconnection approaches the wavelength of the signal (i.e., being transported). For ACL outputs driving transmission lines, the rise time  $t_r$  and the fall time  $t_f$  can be as little as 1.5 nanoseconds. Consequently (from the theory references), printed-circuit board stripline interconnect lengths of about five inches or more should be treated as transmission lines for which either series or shunt terminations may be necessary to preserve system propagation delays. Another way to state this point is that it is desired that all ACL inputs switch on the first or incident pulse edge. Otherwise, a delay of  $t_d$  would be added, where  $t_d$  is the delay of the stripline (about 1.5 nanoseconds per foot).

## Practical ACL Interconnect Design Rules

- Interconnect design rules for both AC and ACT series devices are considered for the following media:
1. Striplines on glass-epoxy printed-wiring boards.
  2. Ribbon cable—single wire and alternate ground wire.
  3. Coaxial cable.

The need for either shunt or series terminations will be illustrated for various interconnect lengths.

## Series Termination

Fig. 30 illustrates the schematic and waveforms for a series termination ( $R_T + R_i = Z_0$ ). This termination faithfully reproduces the IC output pulse with a delay of  $t_d$  the line coming back to the input from the open (unterminated) end of the line is effectively terminated and no further reflections occur. This series termination is very effective for CMOS because the series resistor  $R_T$  does not limit fanout ( $R_i$  of CMOS is nearly infinite). Series termination for TTL logic has a moderate to disastrous effect on fanout and noise

margin because each FAST input draws about 1.8 milliamperes of sink current.

In the waveform of Fig. 30 (b), there is no series termination resistor ( $R_T = 0$  ohms) and reflections bounce back and forth with the result that there is a peak of about 1 volt somewhere in time depending on the line length. In this case the line length is 8 inches. In Fig. 30 (c) waveforms, a 100-ohm series terminating resistor provides a good quality waveform at the end of the line (B) with all areas under 0.8 volt. The fall time is also good. Note the reflection at the (A) falling edge, which is about 3 nanoseconds out, the round-trip delay for the experimental 8-inch stripline board. In Fig. 30 (b), the 300-ohm series resistor  $R_T$  at A clearly makes  $R_T$  greater than the characteristic impedance  $Z_0$ , and the waveform at B has about 8 nanoseconds of added delay because of the large  $R_T$  delay.

# Design Considerations

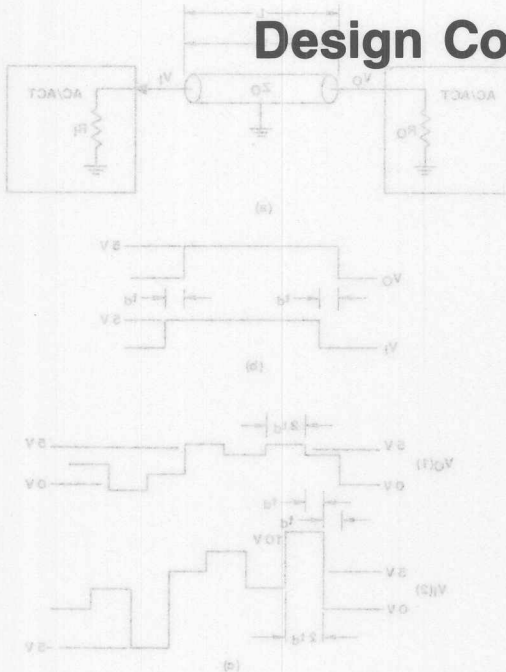


Fig. 29. (a) Basic ACL interconnect environment. (b) Waveforms for ideal situation where  $R_j$  is less than  $Z_0$  and  $R_i$  equals  $Z_0$  (matched). (c) Waveforms for actual "load-word" situation where the interconnection is unterminated. The interconnection length exceeds five inches,  $R_j$  is less than  $Z_0$ , and  $R_i$  is very much greater than  $Z_0$ .

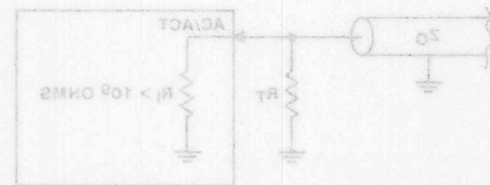


Fig. 30. Line matched by shunt termination resistance  $R_T$  equal to  $Z_0$ . Produces waveforms of Fig. 28 (b).

## INTERCONNECTION OF ACL LOGIC DEVICES

Interconnections of ACL high-speed logic devices by means of single wires, coaxial cable, stripline, ribbon cable, or twisted pair must necessarily be designed to preserve the pulse waveform. Fig. 28 illustrates the basic interconnect environment and shows the pulse waveforms for both the ideal case and the practical or actual case with ACL devices. The ideal case, shown in the waveforms of Fig. 28 (b) when one ACL output port is connected to an input port of another ACL part, is realizable for short interconnect lengths (less than five inches) or for the case when the line is matched by the addition of a shunt termination resistance ( $R_T$ ) in parallel with the input resistance ( $R_I$ ), as shown in Fig. 29.

If the only concern were the fidelity of the pulse waveform at the IC input or load end of the interconnection, which is often but not always the case, then a series termination scheme can be used, as shown in Fig. 30 (a). The resultant waveforms are shown in Fig. 30 (b). This figure shows a very good input pulse waveform at the load-end IC. Here, the value of the series resistor  $R_S$  is selected to make  $R_O$  plus  $R_S$  equal to  $Z_0$ . If the output resistance  $R_O$  is 25 ohms and the characteristic impedance  $Z_0$  is 100 ohms, then  $R_S$  is 75 ohms. This approach is called ideal series matching.

By studying the interconnection environment, the designer quickly learns that if the interconnection distance is "short," there is no concern and the waveforms of Fig. 28 (b) can prevail fairly well. The major design question, however, is what is "short?" Basic interconnect theory, as covered in the references given at the end of this section, states that transmission-line effects or wave effects become an important design consideration when the length of the interconnection approaches the wavelength of the signal ( $f_c$ ) being transported. For ACL outputs driving transmission lines, the rise time  $t_r$  and the fall time  $t_f$  can be as little as 1.5 nanoseconds. Consequently (from the theory references), printed-circuit board stripline interconnect lengths of about five inches or more should be treated as transmission lines for which either series or shunt terminations may be necessary to preserve system propagation delays. Another way to state this point is that it is desired that all ACL inputs switch on the first or incident pulse edge. Otherwise, a delay of  $2t_d$  would be added, where  $t_d$  is the delay of the stripline (about 1.5 nanoseconds per foot).

## Practical ACL Interconnect Design Rules

Interconnect design rules for both AC and ACT series devices are considered for the following media:

1. Stripline on glass-epoxy printed-wiring boards.
2. Ribbon cable—single wire and alternate ground wire.
3. Coaxial cable.

The need for either shunt or series terminations will be illustrated for various interconnect lengths.

## Series Termination

Fig. 30 illustrates the schematic and waveforms for a series termination ( $R_S + R_O = Z_0$ ). This termination faithfully reproduces the IC output pulse with a delay of  $t_d$ , the line delay over length  $L$ . In this interconnection, reflections coming back to the input from the open (unloaded) end of the line are effectively terminated and no further reflections occur. This series termination is very effective for CMOS because the series resistor  $R_S$  does not limit fanout ( $R_I$  of CMOS is nearly infinite). Series termination for TTL logic has a moderate to disastrous effect on fanout and noise

margin because each FAST input draws about 1.6 milliamperes of sink current.

In the waveforms of Fig. 30 (b), there is no series termination resistor ( $R_S = 0$  ohms) and reflections bounce back and forth with the result that there is a peak of about 1 volt somewhere in time depending on the line length. In this case the line length is 8 inches. In Fig. 30 (c) waveforms, a 100-ohm series terminating resistor provides a good quality waveform at the end of the line (B) with all areas under 0.8 volt. The fall time is also good. Note the reflection at the (A) falling edge, which is about 3 nanoseconds out, the round-trip delay for the experimental 8-inch stripline board. In Fig. 30 (d), the 300-ohm series resistor  $R_S$  at A clearly makes  $R_S$  greater than the characteristic impedance  $Z_0$ , and the waveform at B has about 5 nanoseconds of added delay because of the large  $R_S C_L$  delay.

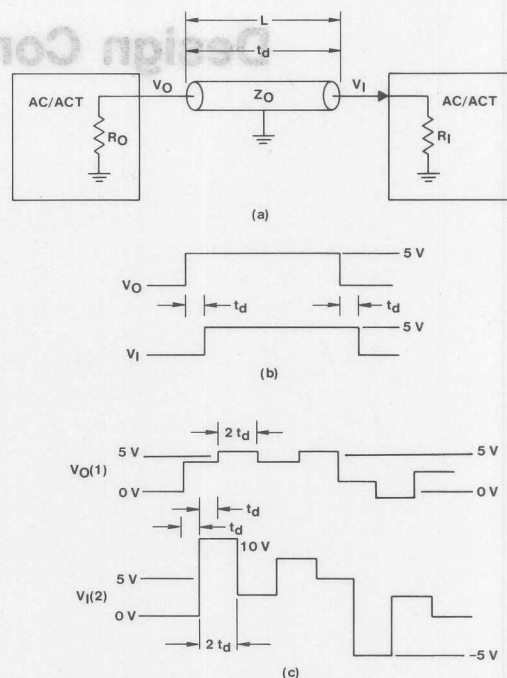


Fig. 28. (a) Basic ACL interconnect environment. (b) Waveforms for ideal situation where  $R_O$  is less than  $Z_0$  and  $R_I$  equals  $Z_0$  (matched). (c) Waveforms for actual "real-world" situation where the interconnection is unterminated, the interconnection length exceeds five inches,  $R_O$  is less than  $Z_0$ , and  $R_I$  is very much greater than  $Z_0$ .

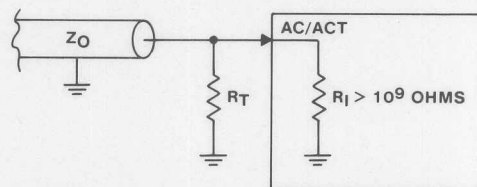


Fig. 29. Line matched by shunt termination resistance  $R_T$  equal to  $Z_0$ . Produces waveforms of Fig. 28 (b).

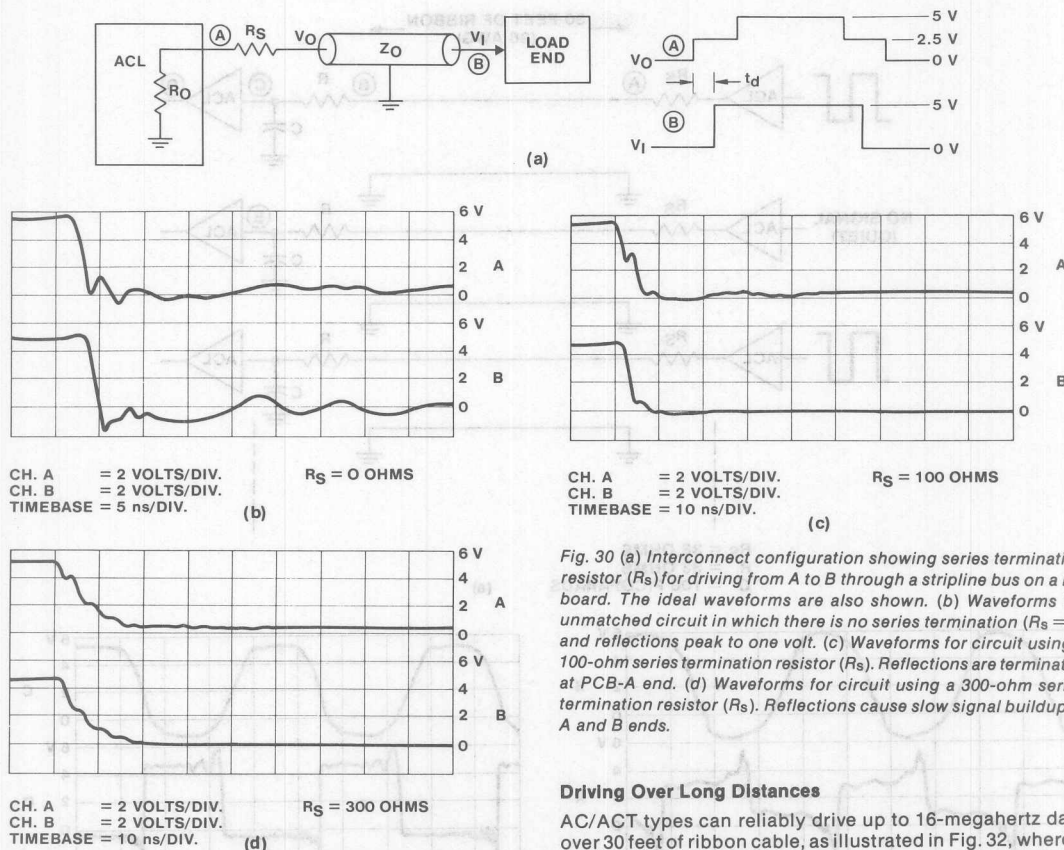


Fig. 30 (a) Interconnect configuration showing series termination resistor ( $R_S$ ) for driving from A to B through a stripline bus on a PC board. The ideal waveforms are also shown. (b) Waveforms for unmatched circuit in which there is no series termination ( $R_S = 0$ ) and reflections peak to one volt. (c) Waveforms for circuit using a 100-ohm series termination resistor ( $R_S$ ). Reflections are terminated at PCB-A end. (d) Waveforms for circuit using a 300-ohm series termination resistor ( $R_S$ ). Reflections cause slow signal buildup at A and B ends.

### Driving Over Long Distances

AC/ACT types can reliably drive up to 16-megahertz data over 30 feet of ribbon cable, as illustrated in Fig. 32, where 5 megahertz is used as an illustration. The series resistor  $R_S$  (33 ohms) is used to terminate the lines. Over the 30-foot distance, although there is some cross coupling of signals (see Fig. 32 waveforms), it is conveniently attenuated with the small RC network at the receiving end inputs. Any AC or ACT type output is a suitable transmitting source, but only AC types should be used at the receiving end. FAST types cannot be used in this situation because they cannot handle the added series resistor  $R_S$  nor do they have the noise immunity required at the inputs. The ribbon cable recommended is No. 28 AWG with the alternate wires grounded as partial cross-coupling shields. Twisted-pair cable would be even better in this long-interconnection arrangement.

As shown in Fig. 31, other bus drivers or receivers may also be connected to a transmission line and load the line incrementally by  $C_i$ , the distributed input capacitance. The net effect is to reduce the  $Z_O$  of the stripline bus as a result of the added  $C_i$ .

$$Z_o = [L_o / (C_o + C_i)]^{1/2}$$

Reflections occur because of the very high  $R_i$  of the ACL devices at B plus the discontinuities caused by the distributed  $C_i$ . A series termination resistor ( $R_S$ ) of the proper value connected right at the ACL driver output pin at A effectively stops the reflection at the A end, and because there is no reflection back down to the B input, there is no undesirable ringing of the line.

A summary of the experimental results for an 8-inch two-sided PC board stripline interconnect of any AC/ACT type follows:

1. For TTL logic levels ( $V_{IL} = 0.8$  volt) using ACT types, a series  $R_S$  of 100 ohms is beneficial and provides for a clean signal at the load or input end of an interconnection. A value between 50 and 100 ohms works well.
2. For CMOS logic levels, no series termination resistor  $R_S$  is needed. Signals stay within the noise immunity levels of AC logic; i.e.,  $V_{ILmax} = 1.5$  volts and  $V_{IHmin} = 3.5$  volts where the typical switching level is 2.5 volts.

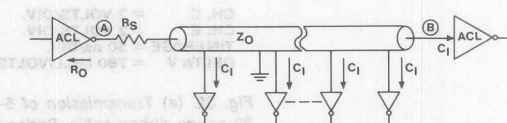


Fig. 31. Transmission line feeding a number of ACL inputs.



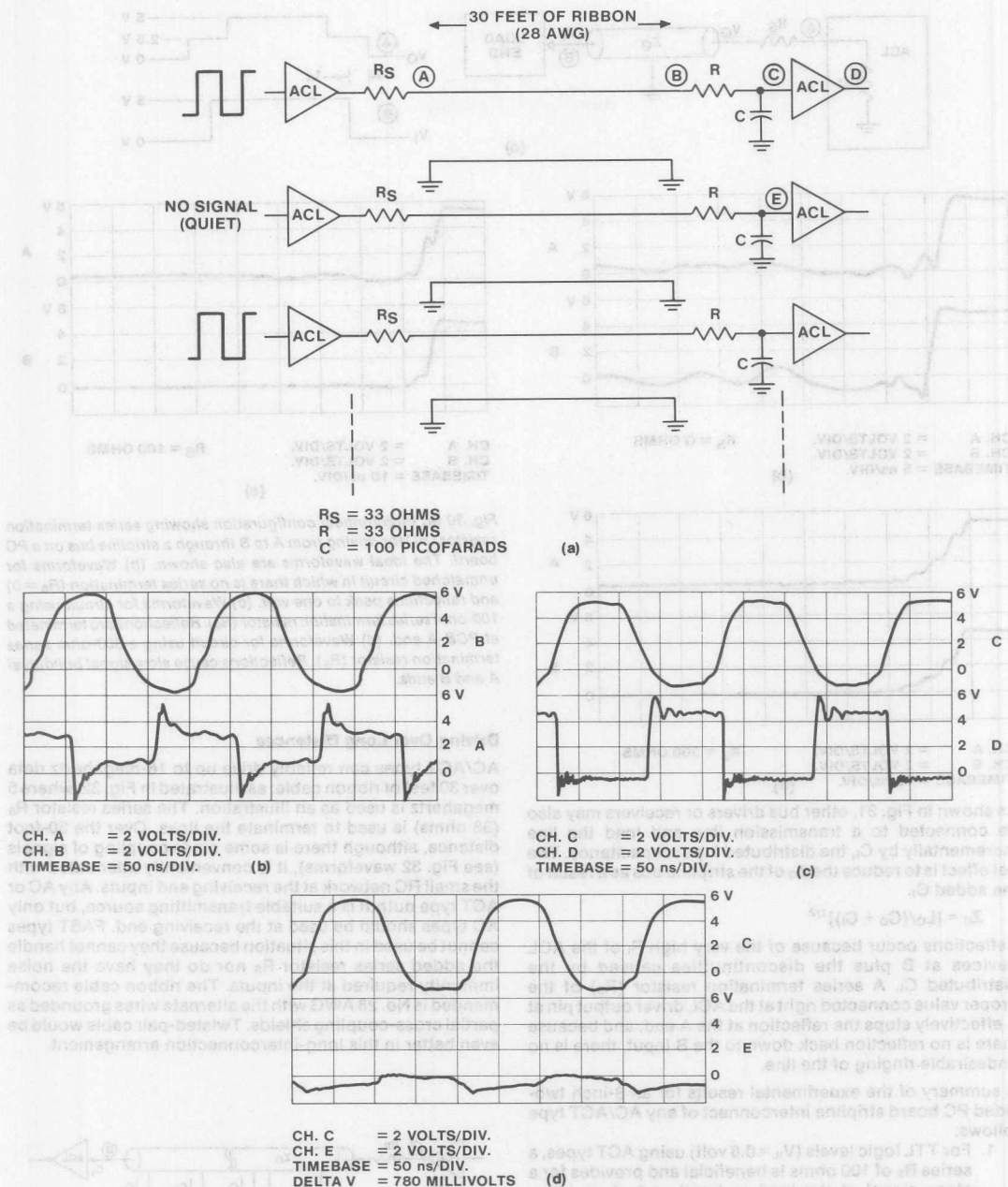


Fig. 32. (a) Transmission of 5-megahertz signal over 30 feet of 28-gauge ribbon cable. Series termination resistor and crosstalk attenuation RC circuit are used. (b) Switched line waveforms at points A and B. (c) Switched line waveforms at points C and D. (d) Crosstalk signal on quiet line E resulting from influence of waveform at point C.

### Shunt Termination

Traditional transmission lines designed for bipolar logic use shunt terminations at the load end to prevent reflections from developing. Fig. 28 (b) shows this termination in an ideal situation. For ACL logic this interconnection is achieved by the insertion of a resistive shunt termination  $R_T$  right at the inputs, as shown in Fig. 33. It should be remembered that AC/ACT inputs are of nearly infinite resistance. This situation is very favorable for AC/ACT logic devices because the  $R_i$  of the device does not influence  $R_T$  or unbalance the results. This advantage does not exist for bipolar FAST devices. For these types, the  $R_i$  for logic low levels is under 2 kilohms and for high-level signals it is over 7 kilohms.

The example shown in the Fig. 34 test circuit and the waveforms in Fig. 33 (b) illustrate how excellent ACT input-signal integrity can be achieved. Note that all reflections are kept below 0.8 volt ( $V_{IL}$  of TTL and ACT types). In order to reduce the extra 40 milliwatts of power that this resistive termination generates, 50 milliwatts can be eliminated by blocking the direct current flow to ground with a 0.1-microfarad blocking capacitor in series with the 470-ohm resistor of Fig. 34.

When AC types are used as input (line receiver) devices, an outstanding advantage is achieved. This advantage is that no shunt termination is required to achieve incident wave-edge switching at both ends of a transceiver interconnection, as shown in Fig. 35 (a). In Fig. 35 (b), a plot of the incident-edge signal at the drivers on either end shows that the output resistance of the AC types is low enough to attenuate reflections coming back from unterminated loads through a 50-ohm transmission line. Note that the  $V_{OL}$  of 1.65 volts and the  $V_{OH}$  of 3.85 volts meet the 30 per cent noise immunity criteria for AC types.

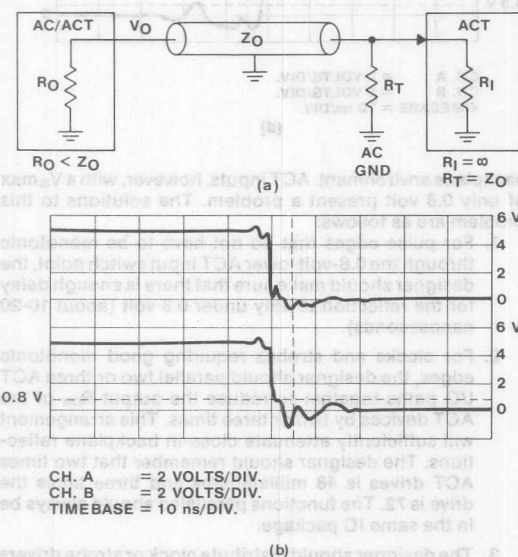


Fig. 33. (a) ACL circuit using shunt termination resistor  $R_T$  equal to  $Z_O$ . (b) Waveforms maintain integrity.

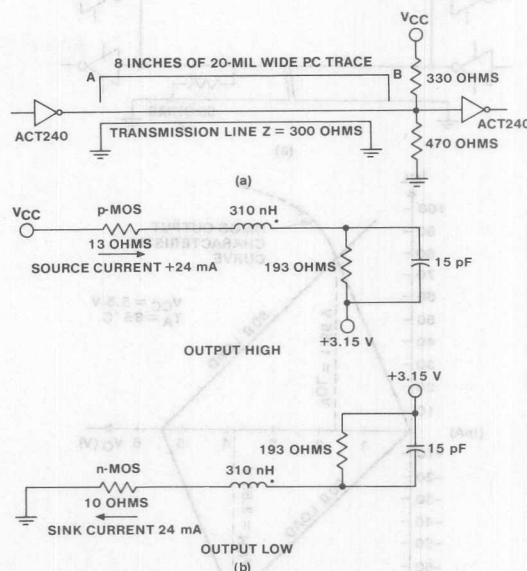


Fig. 34. (a) Stripline interconnection with VME termination at receive end. (b) Equivalent circuits.

Fig. 35 performance is valid for temperatures up to 85°C. Between 85°C and the maximum temperature value of 125°C, the transmission line  $Z_O$  must be 75 ohms or more. Each AC/ACT data sheet provides the additional high-current specification, which guarantees this performance capability; i.e. drive 50- to 75-ohm lines without power-absorbing terminations. The waveform of Fig. 35 (c) illustrates that for eight inches of two-sided board stripline, no terminations are necessary for AC types. However, for this poor type of stripline (two-sided board) the significant inductance of the PC trace causes RLC ringing that barely stays below 1.5 volts, the limiting  $V_{IL}$  for AC inputs. The simple addition of a 470-ohm shunt termination resistance to ground dampens the ringing to 1.1-volts peak, leaving a 0.4-volt noise margin. See Fig. 35 (d). With the 470-ohm termination at the input, this line could be 12 inches or more. For a transceiver type, the 470-ohm resistor would be used at both ends of the line. If a multilayer board is used to produce an interconnect having a lower characteristic impedance, the ringing would be much less than shown in Fig. 35 (c). Longer unterminated interconnections (more than eight inches) are reliable.

### Effects of Distributed Taps on a Bus Line

Under the heading Series Termination, the subject of distributed AC/ACT taps was briefly discussed. Because the use of taps is a common practice, such as the 21 I/O ports for each of the 21 possible cards in a fully populated VME backplane, the effects and the design remedies require attention. It is recalled that an ideal transmission line produces perfectly shaped waveforms at the transmit and receive end, as shown in Fig. 28 (b). In Fig. 36 (a), a VME backplane having 21 I/O ports is depicted. Each ACL I/O port is represented by a net capacitance (see Fig. 36 (b)) of about 20 picofarads, including the IC port, PC board stripline, and connector pin capacitance. This net capacitance can easily reduce  $Z_O$  by about 2/3 from 100 ohms to 33

ohms. The upper sketched waveform of Fig. 36 (c) depicts how the mismatched line produces a pulse of reduced amplitude for  $2t_d$  (the round-trip delay time of the line). By changing the value of termination resistor  $R_T$  to 66 ohms at each end of the line, the shape of the line pulse waveform is restored to its desired rectangular form, the lower waveform in Fig. 36 (c). The full amplitude swing is also reduced, however, because the net resistive load seen by the AC/ACT driver is 33 ohms.

...the ... ..

1. For pulse edges that do not have to be monotonic through the 0.8-volt lower ACT input switch point, the designer should make sure that there is enough delay for the reflection to stay under 0.8 volt (about 10-20 nanoseconds).

2. For clocks and strobes requiring good monotonic edges, the designer should parallel two or three ACT I/O paths together to reduce the output  $R_{ON}$  of the ACT devices by two or three times. This arrangement will sufficiently attenuate close-in backplane reflections. The designer should remember that two times ACT drives is 48 milliamperes and three times the drive is 72. The functions paralleled should always be in the same IC package.
3. The designer should distribute clock or strobe drivers in the same IC package as shown in Fig. 37 to further reduce reflections and produce excellent monotonic edge performance.

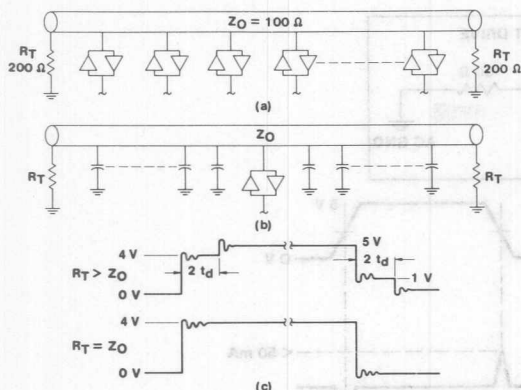


Fig. 36. Distributed AC/ACT loads on a transmission line. (a) AC/ACT transceiver with 21 I/O ports connected to VME backplane. (b) AC/ACT I/O ports look like a pure capacitive load that changes the effective  $Z_0$  of the line. (c) Waveforms for  $R_T$  greater than  $Z_0$  and for  $R_T$  equal to  $Z_0$ .

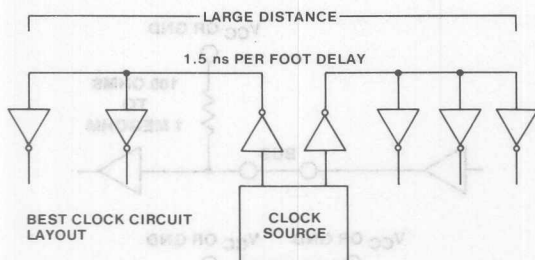


Fig. 37. Recommended distribution of clock or strobe drivers.

### Simultaneous Switching Transients for Driving Transmission Lines

Fig. 38 illustrates that when an ACL output device drives a 100-ohm transmission line, it really looks into a 50-ohm resistive load (two parallel 100-ohm branches of the line with  $Z_0 = 100$  ohms). The waveform of Fig. 38 shows that a peak switching transient of under 50 milliamperes is drawn for two or three nanoseconds. In a worst-case situation, an octal device with eight outputs switching simultaneously could theoretically draw  $8 \times 50$  milliamperes or 0.4 ampere. Although 0.4 ampere is a lot of current for a high-frequency-content transient, it is under the peak switching current developed by the direct drive of a pure 50-picofarad capacitive load (a worst case). The "real world" of backplane or bus systems is an instantaneous 50- to 150-ohm resistive transmission-line load as depicted in Fig. 38. If the effects of simultaneous switching are applied to this load, the induced voltage transient ( $V_{OLP}$ ) on the eighth unswitched output would be less than one volt.

### Min/Max Propagation Delay and Delay Skew

The designer of bus interfaces, or bus protocols, has many considerations for reliable bus or backplane data handling. The ideal goal is a logic level error probability of 0 per cent.

One of the most critical and system-speed-limiting parameters is worst-case min/max propagation delay. This parameter considers data-sheet-guaranteed min/max delay as a function of supply voltage  $V_{CC}$ , temperature, distributed capacitance, and high/low transitions. This variation in I/O delays must also consider simultaneous switching delay skew; i.e., the  $t_{PLH}/t_{PHL}$  for one output of an octal bus interface type compared to values when all eight outputs simultaneously switch. As mentioned earlier, simultaneous switching lifts the output driver ground reference and also lowers the instantaneous  $V_{CC}$  reference level. This change momentarily reduces gate-to-source voltage, reduces  $g_m$ , and produces an increase in  $R_{ON}$  in MOS transistors. Thus, the bigger the output stage RC delay, the bigger the change in  $t_{PLH}/t_{PHL}$ .

Information on min/max delay variations of ACL devices follows:

1. All ACL data sheets provide the design engineer with one min and max delay limit for  $t_{PLH}$  and  $t_{PHL}$ . Unlike the designed-in unbalanced value for bipolar FAST types, the same value applies to both  $t_{PLH}$  and  $t_{PHL}$ . This value is for worst-case voltage, min/max voltage, and min/max worst-case temperature conditions.  $C_L$  is pegged at 50 picofarads. The data sheets have supply voltage entries at 1.5,  $3.3 \pm 0.3$ , and  $5 \pm 0.5$  volts. Fig. 23 in the **Technical Overview Section** shows a curve of normalized delay as a function of  $V_{CC}$  variation for all AC/ACT types. Fig. 22 shows delay as a function of  $C_L$ , and Fig. 24 shows delay as a function of temperature.
2. Simultaneous switching delay skew for ACL types is relatively small because of the extensive chip and package features of the GE/RCA AC/ACT product that reduce  $V_{CC}$  and ground bounce to a minimum. Although the data given in Table VIII is only a sample of skew data, it is representative because all AC/ACT interface types have the same output stage and  $V_{CC}$ /ground distribution features.

### Input Terminations

This section discusses the termination of used and unused inputs to ACL devices.

**Unused Inputs** are terminated as shown in Fig. 39 (a). Logic inputs for non-I/O ports should be terminated to  $V_{CC}$  or ground with or without a resistor. The value of the resistor can range from 0 to one megohm. I/O or transceiver ports should be terminated to  $V_{CC}$  or ground only by means of a resistor of 100 ohms minimum to one megohm maximum, as shown in Fig. 39 (b). The consideration here is that if the port is in the driver mode, short to  $V_{CC}$  or ground must be avoided.

**Used Inputs** are terminated as shown in Fig. 39 (c). There are application situations in which an input may become a floating one when system power is on. An example is for CMOS inputs coming off an edge card connector. If the card driving a particular bus line is pulled, then the CMOS input at the receiving PC card input becomes floating. The rule here is to terminate such inputs to  $V_{CC}$  or ground with a resistor 100 ohms to one megohm in value. If the interconnection is a terminated bus, however, such as a terminated VME backplane, individual input terminations such as those shown in Fig. 39 (c) are not required.



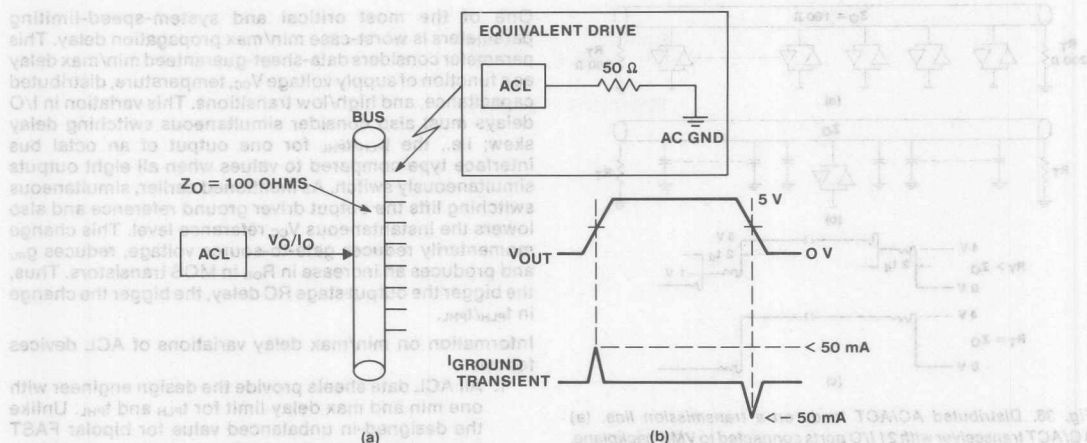


Fig. 38. Current transient caused by line driving. (a) Circuit. (b) Waveform.

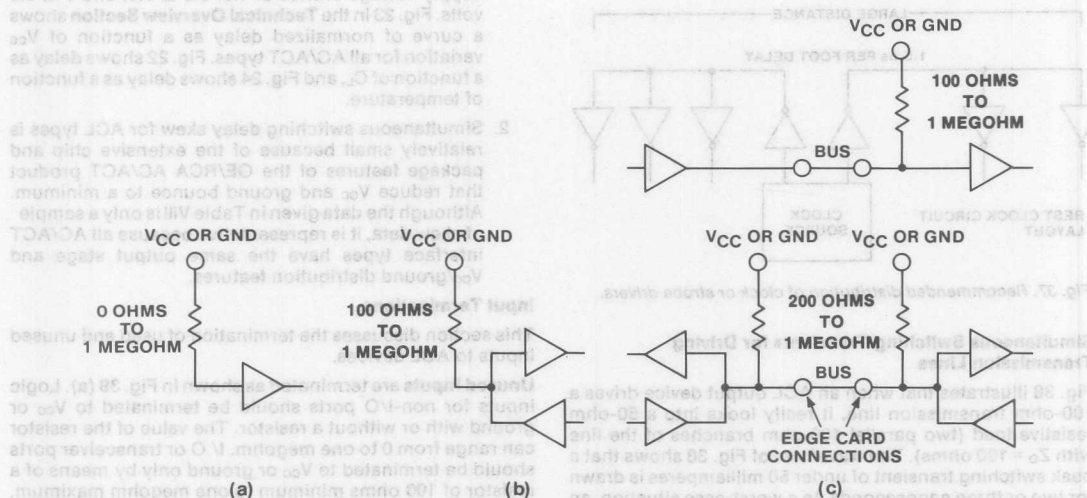


Fig. 39. Input terminations for (a) unused logic inputs, (b) unused I/O ports inputs, and (c) used inputs coming off an edge card connector.

#### Insertion and Removal of Live PC Boards.

"Live" insertion refers to the plugging in of a PC board or daughter card into an electrically live bus, backplane, or mother board. The designer using ACL logic devices should assume that some bus activity may be electrically disrupted momentarily because of interference at plug in. Live removal merits the same considerations. Fig. 40 shows the electrical circuit for ACL types that could momentarily disrupt a bus line. If either the input or output pin of an ACL bus driver/receiver at the PC board interface to the bus touches the bus before  $V_{CC}$  makes contact, the entire PC

board takes power off the bus line, if it is in the high state. This action would bring the  $V_{IH}$  level under the  $V_{IHmin}$  value, and thus the signal level on the bus would be non-determinate until the  $V_{CC}$  pin completes contact. If a system designer requires live insertion without fault tolerance, the most reliable design solution is for PC boards to have longer pins for  $V_{CC}$  and ground. This difference in pin lengths assures that the diodes of Fig. 40 will not momentarily conduct. Because of the latch-up-free production process and circuitry, as discussed earlier, no harm to ACL ICs occurs if the I/O protection diodes momentarily conduct.

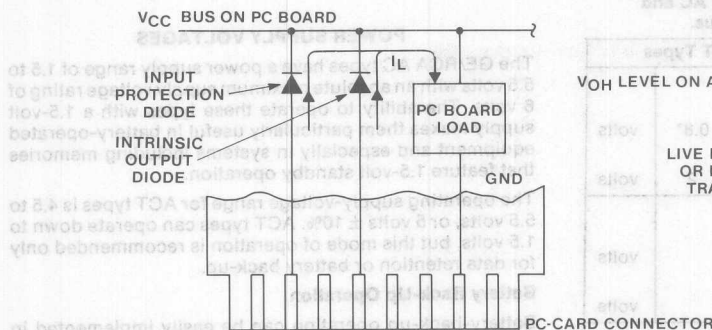


Fig. 40. ACL I/O clamp diodes can momentarily pull down a high state on a bus.

### Bus Contention

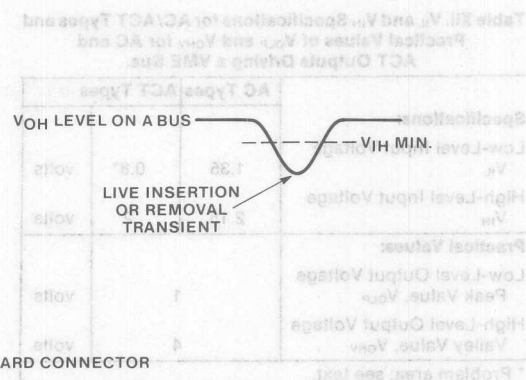
When more than one driver is connected to a bus, which is usually the case as illustrated in Fig. 41, contention could occur. Considering the actual min/max spread of IC logic line delays and the differences in interconnect delays (delays are approximately 1.5 nanoseconds per foot), it is not surprising that bus contention among drivers could occur.

Fig. 42 shows the bus contention delay waveforms for all AC/ACT 2- or 3-state output devices, except for the open-drain types. The separate waveforms for AC and ACT types are shown and compared to bipolar FAST types. Because of the well balanced AC/ACT output drive ( $I_{OL} \approx I_{OH}$ ), bus contention gives a possible mid-state delay of typically a few nanoseconds or in the worst case ( $t_{max} - t_{min}$ ) about seven nanoseconds. For comparison, bipolar FAST bus drivers have the same worst-case delay for the low-to-high-state changes, but the much heavier sink current (48 to 64 milliamperes) keeps  $V_{OL}$  below  $V_{IH}$ . Good IC decoupling is essential because, at the momentary  $V_{CC}/2$  level, up to 100 milliamperes could flow from  $V_{CC}$  to ground. This condition is an example of where ACT types provide superior bus performance because of their  $V_{IHmin}$  value of two volts.

A good solution to contention problems is the use of the AC/ACT open-drain types as bus drivers. Types suggested include the following:

AC/ACT 05	Hex Inverter with Open-Drain Outputs
AC/ACT 647/649	Octal Bus Transceiver Register With Open Drain
AC/ACT 653/654	Octal Bus Transceiver Register, Open Drain A Side, 3-State B Side
AC/ACT 7623	Octal Bus Transceiver, Open Drain A Side, 3-State B Side, Non-Inverting

With these types, not only is bus contention eliminated, but a very useful form of bus logic, called "bus wired-OR" can be used. Bus arbitration design problems are also resolved by the use of the wired-OR. Most bus designs use wired-OR for some lines, but with proper design it could be used for most or all lines so long as the pull-up delay ( $t_{PLH}$ ) due to the use of resistive bus-termination networks is not excessive for the speed of the system.



### Bus Drivers

Individual ACL bus drivers connected to a VME bus, multibus, or other electrical backplane may have the edge waveforms shown in Fig. 43. Each bus tap has a net capacitance that ordinarily disrupts transmission line performance and produces reflections with undesirable  $V_{OLP}$  and  $V_{OHV}$  signals, as shown in the waveforms of Fig. 43.  $V_{OLP}$  and  $V_{OHV}$  are the peak and valley values of  $V_{OL}$  and  $V_{OH}$ , respectively. If the value of  $V_{OLP}$  exceeds the logic  $V_{IL}$  or goes below  $V_{OL}$ , a logic error is possible. Table XII reviews the specifications for AC and ACT types and shows practical values of  $V_{OLP}$  and  $V_{OHV}$  for AC and ACT outputs driving a well-populated VME bus. The problem area, emphasized in the Table, is the  $V_{IL}$  for TTL logic levels applicable to ACT or to any bipolar FAST device because  $V_{OLP}$  is greater than  $V_{IL}$ .

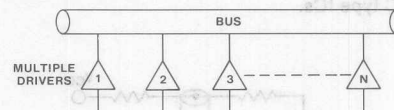


Fig. 41. Multiple bus drivers.

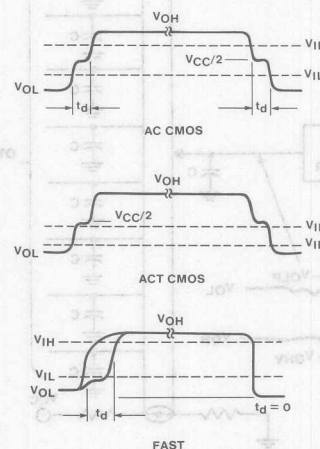


Fig. 42. Bus contention delay waveforms for AC and ACT CMOS types and for bipolar FAST types.

**Table XII.  $V_{IL}$  and  $V_{IH}$  Specifications for AC/ACT Types and Practical Values of  $V_{OLP}$  and  $V_{OHV}$  for AC and ACT Outputs Driving a VME Bus.**

Specifications:	AC Types	ACT Types	
Low-Level Input Voltage $V_{IL}$	1.35	0.8*	volts
High-Level Input Voltage $V_{IH}$	2.15	2	volts
<b>Practical Values:</b>			
Low-Level Output Voltage Peak Value, $V_{OLP}$		1	volts
High-Level Output Voltage Valley Value, $V_{OHV}$		4	volts

\* Problem area; see text.

There are several solutions to this problem. For applications of ACT types where there are data/address or non-edge-sensitive lines, the user should allow a bus settling time of 10 to 20 nanoseconds. For clocks or strobes where monotonic edges are important, the designer should increase the output device drive current by paralleling two or three (three is best but more is satisfactory) inputs and outputs of the bus interface logic functions, as shown for the AC/ACT 240 type in Fig. 44. It is very important that the paralleled functions all be in the same IC package.

For applications of AC types, this problem does not exist because the superior input noise immunity of these types gives sufficient noise margin. The fastest and most reliable (compared to ACT or FAST/AS/S type applications) bus system designs are achieved with the advanced high-speed CMOS AC type ICs.

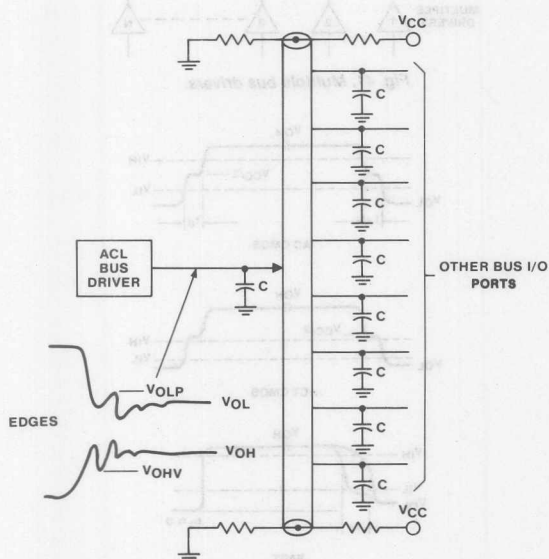


Fig. 43. AC/ACT bus driver circuit and edge waveforms.

## POWER SUPPLY VOLTAGES

The GE/RCA AC types have a power supply range of 1.5 to 5.5 volts with an absolute maximum supply voltage rating of 6 volts. The ability to operate these types with a 1.5-volt supply makes them particularly useful in battery-operated equipment and especially in systems including memories that feature 1.5-volt standby operation.

The operating supply-voltage range for ACT types is 4.5 to 5.5 volts, or 5 volts  $\pm 10\%$ . ACT types can operate down to 1.5 volts, but this mode of operation is recommended only for data retention or battery back-up.

## Battery Back-Up Operation

Battery-back-up operation can be easily implemented in systems containing ACL devices. An example of such an arrangement is given in Fig. 45. The minimum battery voltage required is only 1.5 volts plus the voltage drop of one diode. Schottky diodes should be used because of their very low voltage drop (typically 0.2 volt). In Fig. 45, GE/RCA High-to-Low Level Shifters HC4049 or HC4050 are used to prevent the flow of positive input currents into the system in the event of input voltage levels greater than one diode voltage drop above  $V_{cc}$ . These types do not have clamp protective devices at the  $V_{cc}$  inputs. More information on this subject can be obtained from ICAN-7373, Logic Designs for Battery-Powered or Battery-Backed-Up Operation.

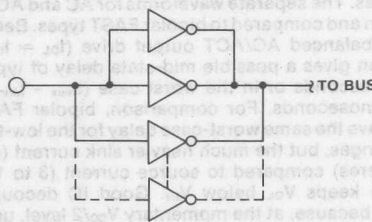


Fig. 44. Paralleled AC/ACT functions must be in same IC package only.

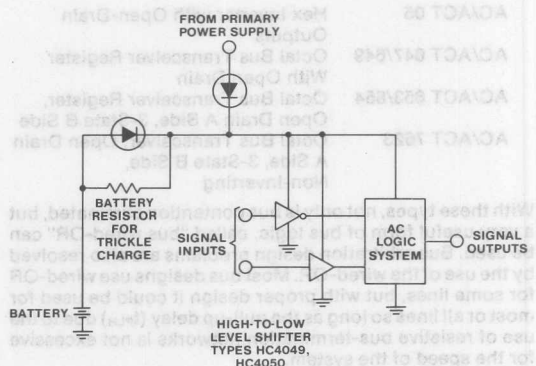


Fig. 45. Example of AC/ACT system with battery back-up.

### Power Supply Regulation and Decoupling

The wide power supply range of 1.5 to 5.5 volts for AC devices may suggest that regulation is not necessary. But, it must be realized that a changing supply voltage affects system speed, noise immunity, and power consumption. Because noise immunity and even the correct operation of the circuit can be affected by noise spikes on the supply lines, matched decoupling is always necessary in dynamic systems.

AC and ACT types both have the same power supply regulation and decoupling requirements. The best method of minimizing spiking on the supply lines is by implementing good power supply and ground busing and by having low ac impedances from the  $V_{CC}$  and ground pins of each device. Because the minimum value of a decoupling capacitor depends on the voltage spikes that can be allowed, it is a general rule to restrict ground and  $V_{CC}$  noise peaks to 100 millivolts. A local voltage regulator on the printed-circuit board can be decoupled by means of an electrolytic capacitor of 10 to 50 microfarads.

The selection of a bypass capacitor for an Octal Driver types falls into one of the cases listed below. The equation for all three cases is

$$C_{\text{bypass}} = 8 I_{\text{peak}} \Delta t / \Delta v$$

#### 1. Worst-Case Pure Capacitance Load

$I_{\text{peak}}$  = short-circuit current for an AC/ACT output (200 milliamperes)

$\Delta t$  = 6 nanoseconds for a load of up to 300 picofarads

$\Delta v$  = 0.1 volt (assumed drop allowed)

$$C_{\text{bypass}} = (8)(0.2)(6 \times 10^{-9}/0.1) \\ = 96 \text{ nanofarads}$$

The practical value to use is 0.1 microfarad.

#### 2. Average Stripline Drive

$Z_o$  = 300 ohms

$I_{\text{peak}}$  = 5 volts/150 ohms = 33 milliamperes

$\Delta t$  = 2 nanoseconds

$\Delta v$  = 0.1 volt

$$C_{\text{bypass}} = (8)(33 \times 10^{-3})(2 \times 10^{-9}/0.1) \\ = 5.3 \text{ nanofarads}$$

The practical value to use is 0.0056 microfarad.

#### 3. Driving resistive load (100-ohm transmission line)

$Z_o$  = 100 ohms (two branches in parallel is 50 ohms)

$I_{\text{peak}}$  = 5 volts/50 ohms = 0.1 ampere

$\Delta t$  = 3 nanoseconds

$\Delta v$  = 0.1 volt

$$C_{\text{bypass}} = (8)(0.1)(3 \times 10^{-9}/0.1) \\ = 24 \text{ nanofarads}$$

The practical value to use is 0.01 microfarad.

For each case, the designer should keep the lead lengths of the capacitors very short and use good quality radio-frequency capacitors such as class 1 monolithic ceramic types. These types are very low loss at high frequencies and over a wide temperature range.

### INTERFACING

#### Interfacing with ACL Logic

ACT logic, like the slower HCT logic, is the most versatile logic family available for interfacing between any CMOS or TTL logic-level devices, as shown in Fig. 46. The only restrictions are the input rise and fall slew rates (see AC/ACT data sheets). If the maximum rise or fall slew rate of the CMOS or TTL output is too slow, the AC/ACT14 or HC/HC14 Hex Schmitt Trigger types are available and should be used to speed up slow output pulse edges. Note in Fig. 46 that ACT logic devices also accept NMOS logic levels.

Fanout restrictions to AC/ACT or TTL logic families are discussed in the **Technical Overview Section** of this Databook.

AC types, as shown in Fig. 46, cannot be directly driven from any of the TTL families because the TTL output voltage high,  $V_{OHmin}$ , does not satisfy the AC input voltage high,  $V_{IHmin}$ , specification. To meet minimum  $V_{IH}$  requirements, AC types, however, can use a pull-up resistor, as illustrated in Fig. 47, to accept TTL logic-level inputs reliably.

Interfacing AC/ACT logic with ECL logic is an important application requirement because of the very high speed of AC/ACT. Fig. 48 illustrates use of available ECL to TTL logic transistor types that are applicable to ACT types.

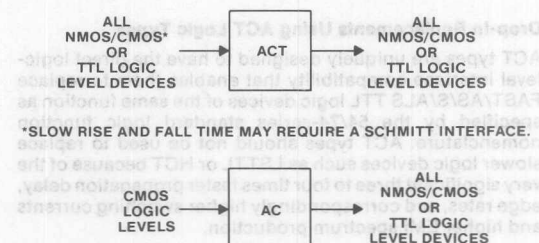


Fig. 46. AC/ACT NMOS/CMOS interfacing using AC and ACT types.

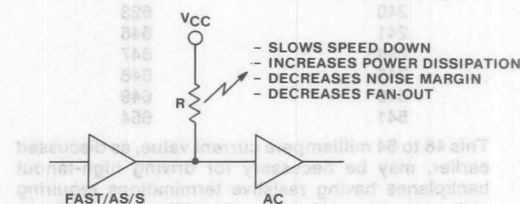


Fig. 47. Use of pull-up resistor to interface TTL and AC devices.



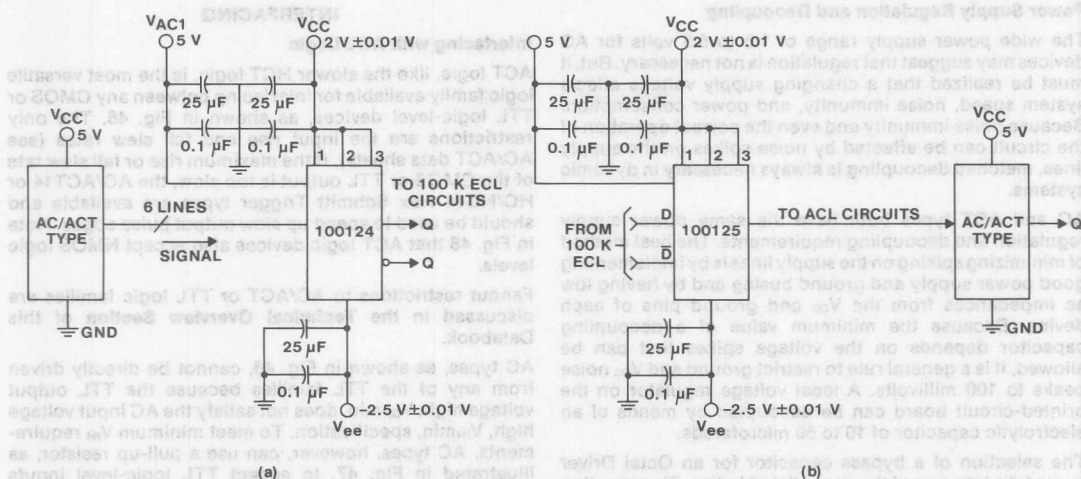


Fig. 48. Use of logic translator types to interface AC/ACT logic with ECL logic. (a) Interfacing AC/ACT to ECL circuits. (b) Interfacing ECL to AC/ACT circuits.

### Drop-In Replacements Using ACT Logic Types

ACT types are uniquely designed to have the direct logic-level interface compatibility that enables them to replace FAST/AS/S/ALS TTL logic devices of the same function as specified by the 54/74-series standard logic function nomenclature. ACT types should not be used to replace slower logic devices such as LSTTL or HCT because of the very significant three to four times faster propagation delay, edge rates, and correspondingly higher switching currents and higher EMI spectrum production.

There are, however, some definite possible limitations to direct drop-in replacement of FAST/AS/S/ALS types with ACT types that must be considered. The considerations are:

1. Certain bus driver types in the FAST or AS family have sink-current capabilities greater than 24 milliamperes; namely, 48 to 64 milliamperes. Types that are in this category include

240	623
241	646
244	647
245	648
540	649
541	654

This 48 to 64 milliampere current value, as discussed earlier, may be necessary for driving high-fanout backplanes having resistive terminations requiring sink currents greater than 24 milliamperes. Clocks and strobe signals are also in this category, as discussed earlier (see Bus Drivers). Consequently, if power is to be saved, some redesign of the printed-circuit board is needed in order to parallel ACT devices within the same package.

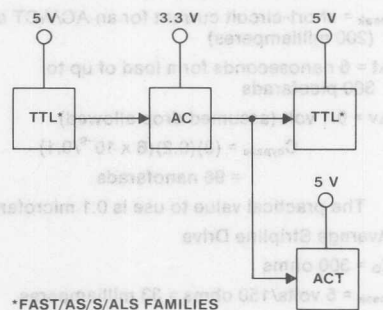


Fig. 49. Use of both 3.3- and 5-volt supplies together.

2. Trace lengths of printed-circuit board interconnections of five inches or more. A good printed-circuit-board design for FAST interconnects of relatively long length should have a shunt termination to achieve good pulse edge fidelity. Because of the high-impedance input of AC/ACT devices ( $R_i$  greater than 100 kilomegohms;  $C_i$  of 7.5 picofarads), more reflected-wave energy can occur than with FAST. Consequently, the addition of 470 ohms of termination resistance to ground directly at the ACT input is recommended.
3. If the FAST types use ribbon cable to interface, the higher input impedance at the receive end may require termination resistance and some small capacitance to ground to reduce crosstalk. When FAST types are used for both the driver and the receiver, it is recommended that ACT types be substituted for the driver and AC types for the receiver. With these substitutions, noise performance results should be much superior to the results with FAST types.

### LOWER-VOLTAGE OPERATION

For CMOS logic "less is best" in terms of all-around optimum system performance. The designer of CMOS logic circuits using AC Devices can make effective use of the broad-range supply-voltage capability (1.5 to 5.5 volts) to

1. Minimize operating power consumption

$$P_{\text{operating}} = CV_{\text{cc}}^2 f$$

2. Minimize switching-current transients into capacitive loads

$$I_{\text{peak}} = C\Delta v/\Delta t$$

3. Minimize EMI spectrum production. Table VII in the **Technical Overview Section** shows how output transition times and, hence, Fourier frequency components are reduced by operation at lower supply voltages.

The equipment designer can use the propagation delays as guaranteed in the data sheets at 1.5 volts or, more importantly, at the new industry standard  $3.3 \pm 0.3$  volts (see references at end of section) to determine if the logic speed needs are being met. Fig. 23 in the **Technical Overview Section**, the curve showing normalized propagation delay as a function of supply voltage, is also very useful in this consideration.

Although these three significant benefits of operating AC logic below 5 volts, namely 3.3 volts, are enticing, there are negatives to consider besides a little slower speed. At 3.3 volts, AC logic has a speed just a bit faster than ALS TTL operating at 5 volts. These negatives are:

1. Five volts is a widely used logic supply voltage and there are many TTL and CMOS logic, microprocessor, and other devices designed for 5-volt use only.
2. Power supplies having both 5-volt and 3.3-volt taps are not currently readily available. Moreover, power supply regulation at 3.3 volts is less efficient than at 5 volts.

The design remedy for the first item above, 5-volt interfacing with TTL, is straightforward, as shown in Fig. 49. AC/ACT data sheets have full dc/ac parameters for  $3.3 \pm 0.3$ -volt operation and such items as sink current for TTL fanouts can easily be accessed.

The solution to the second item above, the lack of  $3.3 \pm 0.3$ -volt regulated supplies, is not so easy to achieve. It requires design innovations through either localized 3.3-volt zener regulation from the 5-volt rail, or power supply design changes to bring out a 3.3-volt tap.

The prognosis for wider use of more optimized 3.3-volt logic or, even further downstream, 2-volt logic is tied heavily into the development of even faster, smaller-geometry CMOS VLSI devices. CMOS devices with features sized at less than one micron can potentially have problems with internal electric fields which, if not remedied by process innovation, may require operation at lower than five volts. Also, the operating power, switching transient production, EMI generation of logic with sub-nanosecond delays also point to the need for operation at lower than five volts. ACL specifications are well poised to provide excellent 1.5- to 5-volt "glue" logic functions and data specifications as this surge to higher-speed, smaller-geometry CMOS goes forward.

### REFERENCES

- Gustafson, D.B., 1984. "Computer Buses—A Tutorial," **IEEE Micro**, August 1984, pp. 7-22.
- Nadolski, J. and Kalish, A., "Using Advanced CMOS Logic in a VME Data Bus System," ICAN-8640.
- Nadolski, J., "Method of Measurement of Simultaneous Switching Transient," ICAN-8754.
- Nadolski, J., "Logic Designs for Battery-Powered or Battery-Backed-Up Operation," ICAN-7373.

The design remedy for the first item above, 5-volt interfacing with TTL, is straightforward, as shown in Fig. 48. AC/ACCT data sheets have full device pinouts for 3.3  $\pm$  0.3-volt operation and such items as sink current for TTL fanouts can easily be assessed.

The solution for the second item above, the lack of 3.3  $\pm$  0.3-volt regulated supplies, is not as easy to achieve. It requires design innovations through either localized 3.3-volt series regulation from the 5-volt rail, or power supply design changes to bring out a 3.3-volt tap.

The prospects for wider use of more optimized 3.3-volt logic are even further downstream. 5-volt logic is tied heavily into the development of even faster, smaller-geometry CMOS VLSI devices. CMOS devices with features sized at less than one micron can potentially have problems with internal electric fields which, if not remedied by process innovation, may require operation at lower than five volts. Also, the operating power, switching transient production, EMI generation of logic with sub-nanosecond delays also point to the need for operation at lower than five volts. AOL specifications are well poised to provide excellent 1.5- to 5-volt "give" logic functions and data specifications as this surge to higher-speed, smaller-geometry CMOS goes forward.

#### REFERENCES

1. Gustafson, D.B., 1984, "Computer Buses—A Tutorial," IEEE Micro, August 1984, pp. 7-22.
2. Hladobski, J. and Keller, A., "Using Advanced CMOS Logic in a VME Data Bus System," ICAN-8840.
3. Hladobski, J., "Method of Measurement of Simultaneous Switching Transient," ICAN-8724.
4. Hladobski, J., "Logic Design for Battery-Powered or Battery-Backed-Up Operation," ICAN-7373.

#### LOWER-VOLTAGE OPERATION

For CMOS logic, less is best, in terms of all-around optimum system performance. The designer of CMOS logic circuits using AC Devices can make effective use of the broad-range supply-voltage capability (1.5 to 5.5 volts) to

1. Minimize operating power consumption.
2. Minimize switching-current transients into capacitive loads.

$$P_{average} = CV_{cc}f$$

3. Minimize EMI spectrum production. Table VI in the Technical Overview shows how output transition times and, hence, Fourier frequency components are reduced by operation at lower supply voltages.

The equipment designer can use the propagation delays as guaranteed in the data sheets at 1.5 volts or, more importantly, at the new industry standard 3.3  $\pm$  0.3 volts (also referenced at end of section) to determine if the logic speed needs are being met. Fig. 20 in the Technical Overview Section, the curve showing normalized propagation delay as a function of supply voltage, is also very useful in this consideration.

Although there are three significant benefits of operating AC logic below 5 volts, namely 3.3 volts, are enticed, there are negatives to consider besides a little slower speed. At 3.3 volts, AC logic has a speed just a bit faster than ALS TTL operating at 5 volts. These negatives are:

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2. Power supplies having both 5-volt and 3.3-volt taps are not currently readily available. Moreover, power supply regulation at 3.3 volts is less efficient than at 5 volts.

# Family Ratings and Specifications

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range, $V_{CC}^{*}$ (For $T_A$ = Full Package-Temperature Range) AO Types ACT Types	1.8	5.5	V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ CDA Types CDB Types	-40	+125	°C
Input Rise and Fall Rate, $dV/dt$ at 1.5 V to 3 V (AO Types) at 3.5 V to 5.5 V (AO Types) at 4.5 V to 5.5 V (ACT Types)	0	30	nA/V
	0	20	nA/V
	0	10	nA/V

\*Unless otherwise specified, all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS:  
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

Absolute Maximum Ratings are those values beyond which damage to the device may occur.  
Functional operation under these conditions is not implied.

\*For up to 4 outputs per device add a 25 nA for each additional output.

Unit: Inserted into P.C. board min. thickness 715 mil. (1.83 mm) with solder contacting lead legs only.  
At distance 715 ± 1.5 mil. (1.83 ± 0.38 mm) from case for 10 s maximum.

LEAD TEMPERATURE (DURING SOLDERING):  
STORAGE TEMPERATURE ( $T_{STG}$ ):  
PACKAGE TYPE E, M: -55 to +125°C  
PACKAGE TYPE F: -55 to +125°C

OPERATING TEMPERATURE RANGE:  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE E)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE F)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE G)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE H)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE J)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE K)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE L)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE M)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE N)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE P)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE Q)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE R)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE S)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE T)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE U)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE V)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE W)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE X)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE Y)  
For  $T_A$  = -55 to +125°C (PACKAGE TYPE Z)

POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):  
DC V<sub>IN</sub> or GROUND CURRENT (I<sub>G</sub> or I<sub>IN</sub>):  
DC OUTPUT SOURCE or SINK CURRENT (I<sub>OL</sub> or I<sub>OH</sub>):  
DC OUTPUT SOURCE or SINK CURRENT (I<sub>OL</sub> or I<sub>OH</sub>):  
DC OUTPUT SOURCE or SINK CURRENT (I<sub>OL</sub> or I<sub>OH</sub>):  
DC INPUT DIODE CURRENT (I<sub>IS</sub> or I<sub>IS</sub>):  
DC SUPPLY VOLTAGE (V<sub>CC</sub>):

MAXIMUM RATINGS: Absolute Maximum Values:  
The absolute maximum ratings, recommended operating conditions, and de-assertion tables of the ACT family are shown on the following pages. Note that the parameter for active only to three-state and other drain device types.

Detailed technical information on each individual type is provided in the technical data section.

## Ratings and Operating Conditions



## Ratings and Operating Conditions

The absolute maximum ratings, recommended operation conditions, and dc specifications tables of the ACL family are shown on the following pages. Note that the parameter  $I_{OZ}$  applies only to three-state and open-drain device types.

Detailed technical information on each individual type is provided in the technical data section.

### MAXIMUM RATINGS, Absolute-Maximum Values:▲

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	.....	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	.....	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	.....	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	.....	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	.....	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):		
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	.....	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	.....	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	.....	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	.....	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	.....	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	.....	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):		
PACKAGE TYPE F	.....	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	.....	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	.....	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	.....	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only	.....	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

▲Absolute-Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

### RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

## Specifications

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS	$V_{CC}$ (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS		
			+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	V <sub>IH</sub>		1.5	1.2	—	1.2	—	1.2	—	V	
			3	2.1	—	2.1	—	2.1	—		
			5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage	V <sub>IL</sub>		1.5	—	0.3	—	0.3	—	0.3	V	
			3	—	0.9	—	0.9	—	0.9		
			5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	3.85	—	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	1.65	—	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current▲	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>									
		V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI†	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

▲3-State devices only (off-state leakage current for open-drain types).

†SSI/FF limits are 4 μA @ +25°C, 40 μA @ 0 to +70°C, -40 to +85°C, 80 μA @ -40 to +125°C (74), -55 to +125°C (54).

A connection must be provided at every input terminal. All unused input terminals must be connected to either  $V_{CC}$  or Gnd, whichever is appropriate.

Output Short Circuits  
Shorting of outputs to  $V_{CC}$  or Gnd may damage CMOS devices by exceeding the maximum device dissipation.

Operating Voltage  
During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients. Power supply ripple, or ground noise, any of these conditions must not cause  $V_{CC}$  — Gnd to exceed the absolute maximum rating.

# Specifications

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current▲	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>		5.5	—	±0.5	—	±5	—	±10	μA
		V <sub>O</sub> = V <sub>CC</sub> or GND									
Quiescent Supply Current, MSI†	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

▲3-State devices only (off-state leakage current for open-drain types).

†SSI/FF limits are 4 μA @ +25°C, 40 μA @ 0 to +70°C, -40 to +85°C, 80 μA @ -40 to +125°C (74), -55 to +125°C (54).

## OPERATING AND HANDLING CONSIDERATIONS

### 1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are similar to those described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

### 2. Operating

#### Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause  $V_{CC} - GND$  to exceed the absolute maximum rating.

#### Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than  $V_{CC}$  nor less than Gnd. Input currents must not exceed 20 mA even when the power supply is off.

#### Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either  $V_{CC}$  or Gnd, whichever is appropriate.

#### Output Short Circuits

Shorting of outputs to  $V_{CC}$  or Gnd may damage CMOS devices by exceeding the maximum device dissipation.

Unit inched into PC board with lead thickness 0.018 in. (0.45 mm) with solder containing lead type only.  $+300^{\circ}\text{C}$   $+300^{\circ}\text{C}$   $+300^{\circ}\text{C}$

Lead temperature (during soldering):

Storage temperature ( $T_{\text{stg}}$ ):

Operating temperature range ( $T_{\text{op}}$ ):

For  $T_{\text{A}} = -40$  to  $+125^{\circ}\text{C}$  (PACKAGE TYPE M)

For  $T_{\text{A}} = -40$  to  $+70^{\circ}\text{C}$  (PACKAGE TYPE N)

For  $T_{\text{A}} = -40$  to  $+125^{\circ}\text{C}$  (PACKAGE TYPE B)

For  $T_{\text{A}} = -40$  to  $+100^{\circ}\text{C}$  (PACKAGE TYPE E)

For  $T_{\text{A}} = -40$  to  $+125^{\circ}\text{C}$  (PACKAGE TYPE F)

For  $T_{\text{A}} = -55$  to  $+100^{\circ}\text{C}$  (PACKAGE TYPE H)

Power dissipation per package ( $P_{\text{D}}$ ):

DC output source or sink current per output pin,  $I_{\text{OL}}$  (for  $V_{\text{OL}} < 0.5\text{ V}$  or  $V_{\text{OH}} > 0.5\text{ V}$ )  $\pm 50\text{ mA}$

DC output diode current,  $I_{\text{OD}}$  (for  $V_{\text{OL}} < 0.5\text{ V}$  or  $V_{\text{OH}} > 0.5\text{ V}$ )  $\pm 50\text{ mA}$

DC input diode current,  $I_{\text{IL}}$  (for  $V_{\text{IL}} < 0.5\text{ V}$  or  $V_{\text{IH}} > 0.5\text{ V}$ )  $\pm 50\text{ mA}$

DC supply voltage ( $V_{\text{CC}}$ ):

MAXIMUM RATINGS, Absolute-Maximum Values:

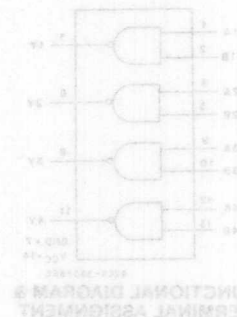
TRUTH TABLE		
INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

FAST is a trademark of Fairchild Semiconductor Corp.

- Output to 15 FAST-ICs
- 24-mA output drive current
- Noise immunity of 30% of the supply
- AC types feature 1.5-V to 5.5-V operation and balanced
- Reduced propagation delays
- Reduced power
- Speed of bipolar FAST-ICs is significantly
- 2CM-L-structure-resistant CMOS process and circuit design
- Method 2015
- ESD Protection - MIL-STD-883

## Technical Data

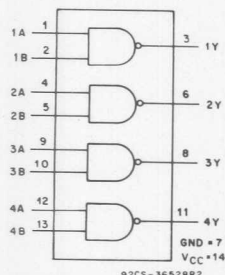
The CD5A7AC00 and CD5A7AC100 are 5-input NAND gates which utilize ADVANCED CMOS LOGIC technology. The CD5A7AC00 and CD5A7AC100 are supplied in 14-lead dual-in-line ceramic packages (E suffix). The CD5A7AC00 and CD5A7AC100 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead small-outline plastic packages (M suffix).



## Quad 5-input NAND Gate

- Type Features:
- Typical propagation delay (AC00):
- 2.5 ns (typical)  $V_{\text{CC}} = 5\text{ V}$ ,  $T_{\text{A}} = 25^{\circ}\text{C}$ ,  $C_L = 50\text{ pF}$





**FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT**

## Quad 2-Input NAND Gate

### Type Features:

- Typical propagation delay (AC00):  
3.2ns @  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50 pF$

The GE/RCA CD54/74AC00 and CD54/74ACT00 are quad 2-input NAND gates which utilize GE/RCA's new ADVANCED CMOS LOGIC technology. The CD54AC00 and CD54ACT00 are supplied in 14-lead dual-in-line ceramic packages (F suffix). The CD74AC00 and CD74ACT00 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).

**TRUTH TABLE**

INPUTS		OUTPUTS
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- $\pm 24$ -mA output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ )	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ )	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ )	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ C$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ C$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ C$ to 300 mW
For $T_A = -40$ to $+100^\circ C$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ C$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ C$ to 300 mW
For $T_A = -40$ to $+70^\circ C$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ C$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ C$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ C$
PACKAGE TYPE E, M	-40 to $+125^\circ C$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ C$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ C$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ C$

\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

# CD54/74AC00 CD54/74ACT00

## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40 -55	+125 +125	°C °C
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types); at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	1.65	—	—	—	
			-50	5.5	—	—	—	—	1.65	—	
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	1.65	—	—	—	
			50	5.5	—	—	—	—	1.65	—	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# CD54/74AC00 CD54/74ACT00

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70		-40 to +125(74)		
							-40 to +85		-55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> #	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> #	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
All	0.15

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# Technical Data

## CD54/74AC00

## CD54/74ACT00

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	$t_{PLH}$	1.5	—	77	—	86	ns
	$t_{PHL}$	3.3*	2	8.7	1.9	9.7	
Power Dissipation Capacitance	$C_{PD}\S$	—	88 Typ.		88 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	$t_{PLH}$	5‡	2.4	11.8	2.3	13.2	ns
	$t_{PHL}$	5‡	2.4	11.8	2.3	13.2	
Power Dissipation Capacitance	$C_{PD}\S$	—	105 Typ.		105 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

‡min. is @ 5.5 V  
max. is @ 4.5 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

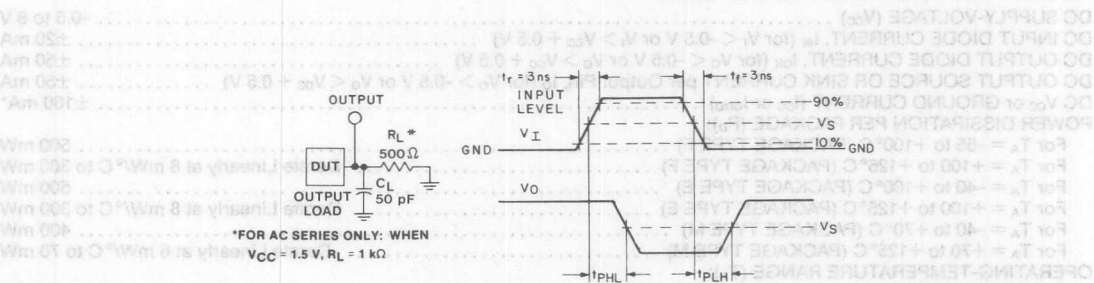
min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§ $C_{PD}$  is used to determine the dynamic power consumption per gate.

For AC,  $PD = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT,  $PD = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage

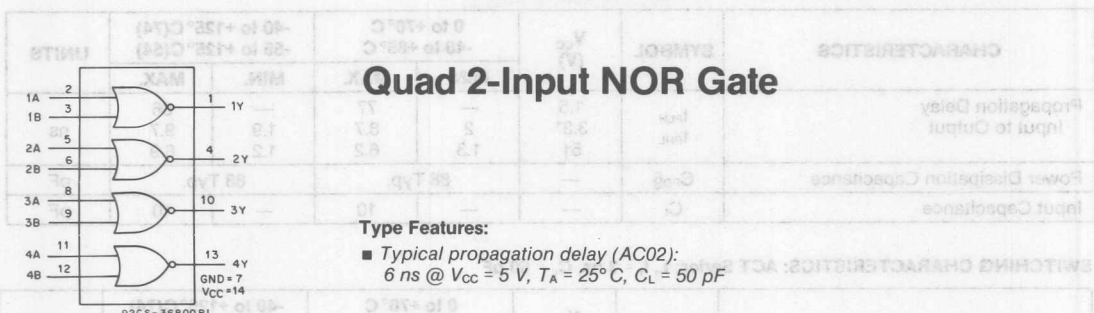


	54/74AC	54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$

Fig. 1 - Propagation delay times.



# CD54/74AC02 CD54/74ACT02



## Quad 2-Input NOR Gate

### Type Features:

- Typical propagation delay (AC02):  
6 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

### FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

The RCA CD54/74AC02 and CD54/74ACT02 are quad 2-input NOR gates that utilize RCA's new ADVANCED CMOS LOGIC technology. The CD54AC02 and CD54ACT02 are supplied in 14-lead dual-in-line ceramic packages (F suffix). The CD74AC02 and CD74ACT02 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).

### TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	H
H	L	L
L	H	L
H	H	L

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC type features 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ )	$\pm 20\text{ mA}$
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ )	$\pm 50\text{ mA}$
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5\text{ V}$ or $V_O < V_{CC} + 0.5\text{ V}$ )	$\pm 50\text{ mA}$
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100\text{ mA}$ *

### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW

### OPERATING-TEMPERATURE RANGE ( $T_A$ ):

PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$

### STORAGE TEMPERATURE ( $T_{stg}$ )

	-65 to $+150^\circ\text{C}$
--	-----------------------------

### LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 $\pm$ 1/32 in. (1.59 $\pm$ 0.79 mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25\text{ mA}$  for each additional output.)

# CD54/74AC02

## CD54/74ACT02

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ : (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40 -55	+125 +125	°C °C
Input Rise and Fall Slew Rate, $dt/dv$ : at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

**STATIC ELECTRICAL CHARACTERISTICS: AC Series**

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5 3.0 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V
Low-Level Input Voltage	V <sub>IL</sub>			1.5 3.0 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	1.5	1.40	—	1.40	—	1.40	—	V
			-0.05	3.0	2.90	—	2.90	—	2.90	—	
			-0.05	4.5	4.40	—	4.40	—	4.40	—	
			-4	3.0	2.58	—	2.48	—	2.40	—	
		# *	-24	4.5	3.94	—	3.80	—	3.70	—	
			-75	5.5	—	—	3.85	—	—	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	1.5	—	0.10	—	0.10	—	0.10	V
			0.05	3.0	—	0.10	—	0.10	—	0.10	
			0.05	4.5	—	0.10	—	0.10	—	0.10	
			12	3.0	—	0.36	—	0.44	—	0.50	
		# *	24	4.5	—	0.36	—	0.44	—	0.50	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		$V_I$ (V)	$I_O$ (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	$V_{IH}$			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	$V_{IL}$			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	4.5	4.40	—	4.40	—	4.40	—	V
		#	-24	4.5	3.94	—	3.80	—	3.70	—	
		*	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.05	4.5	—	0.10	—	0.10	—	0.10	V
		#	24	4.5	—	0.36	—	0.44	—	0.50	
		*	75	5.5	—	—	—	1.65	—	—	
		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	$I_i$	$V_{CC}$ or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI	$I_{CC}$	$V_{CC}$ or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load		$\Delta I_{CC}$	$V_{CC}$ -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE									
INPUT					UNIT LOAD*				
ALL					0.32				
V	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—
V	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—
μA	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC02 CD54/74ACT02

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°		-40 to +125(74) -55 to +125(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	$t_{PLH}$ $t_{PHL}$	1.5 3.3* 5†	— 3.1 2.1	129 14.4 10.3	— 3 2	144 16.1 11.5	ns
Power Dissipation Capacitance	$C_{PD}$	—	—	—	—	—	pF
Input Capacitance	$C_I$	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125(74) -55 to +125(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	$t_{PLH}$ $t_{PHL}$	5†	2.2	10.9	2.1	12.2	ns
Power Dissipation Capacitance	$C_{PD}$	—	—	—	—	—	pF
Input Capacitance	$C_I$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

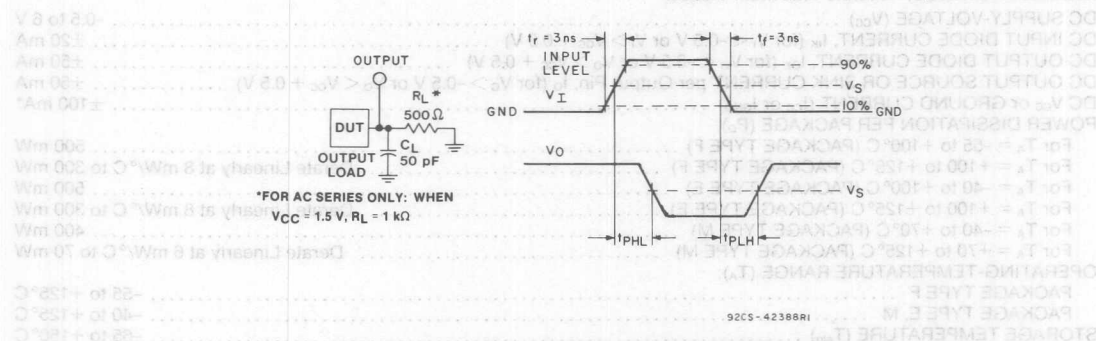
$\$C_{PD}$  is used to determine the dynamic power consumption, per gate.

For AC series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency

$C_L$  = output load capacitance

$V_{CC}$  = supply voltage.

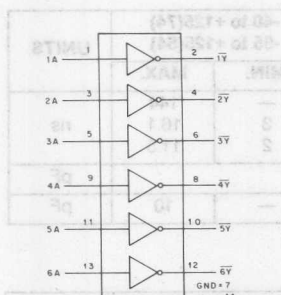


	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$

Fig. 1 - Propagation delay times and test circuit.



# CD54/74AC04, CD54/74AC05 CD54/74ACT04, CD54/74ACT05



## Hex Inverters

CD54/74AC/ACT04 - Active Outputs  
CD54/74AC/ACT05 - Open-Drain Outputs

### FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

The GE/RCA-CD54/74AC04, -05 and CD54/74ACT04, -05 are hex inverters that utilize GE/RCA's new ADVANCED CMOS LOGIC technology. The CD54/74AC/ACT04 have active outputs; the CD54/74AC/ACT05 have open-drain outputs.

The CD54AC04, -05 and CD54ACT04, -05 are supplied in 14-lead dual-in-line ceramic packages (F suffix). The CD74AC04, -05 and CD74ACT04, -05 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).

### TRUTH TABLES

CD54/74AC/ACT04		CD54/74AC/ACT05	
INPUT	OUTPUT	INPUT	OUTPUT
A	Y	A	Y
L	H	L	Z
H	L	H	L

Z = High Impedance

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST<sup>®</sup>/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- ± 24-mA output drive current
  - Fanout to 15 FAST<sup>®</sup> ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	±50 mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	±100 mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{STG}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add ± 25 mA for each additional output.)

# CD54/74AC04, CD54/74AC05

## CD54/74ACT04, CD54/74ACT05

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40 -55	+125 +125	°C °C
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

**STATIC ELECTRICAL CHARACTERISTICS: AC Series**

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>		1.5	1.2	—	1.2	—	1.2	—	V	
			3	2.1	—	2.1	—	2.1	—		
			5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage	V <sub>IL</sub>		1.5	—	0.3	—	0.3	—	0.3	V	
			3	—	0.9	—	0.9	—	0.9		
			5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage (04)	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	V	
			-0.05	3	2.9	—	2.9	—	2.9		—
			-0.05	4.5	4.4	—	4.4	—	4.4		—
			-4	3	2.58	—	2.48	—	2.4		—
			-24	4.5	3.94	—	3.8	—	3.7		—
			-75	5.5	—	—	3.85	—	—		—
			-50	5.5	—	—	—	—	3.85		—
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# CD54/74AC04, CD54/74AC05 CD54/74ACT04, CD54/74ACT05

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70		-40 to +125(74)		
							-40 to +85		-55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage (04)	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	3.85	—		
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load		ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

### ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
nA	0.18

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

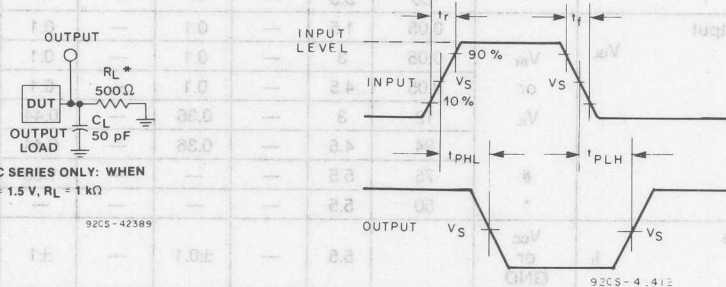


Fig. 1 - Propagation delay times and test circuit - AC/ACT04.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$

# CD54/74AC04, CD54/74AC05

## CD54/74ACT04, CD54/74ACT05

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ 

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C (74) -55 to +125°C (54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	(04)	$t_{PLH}$	1.5	75	—	82	ns
		$t_{PHL}$	3.3*	8.5	1.7	9.1	
			5†	6	1.1	6.5	
High Z to Output Low	(05)	$t_{PZL}$	1.5	75	—	82	ns
			3.3	9	1.7	9.8	
			5	6	1.1	6.5	
Output Low to High Z	(05)	$t_{PLZ}$	1.5	94	—	103	ns
			3.3	9.4	2.1	10.3	
			5	7.5	1.4	8.2	
Power Dissipation Capacitance	$C_{PD}\S$	—	105 Typ.		105 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ 

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C (74) -55 to +125°C (54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	(04)	$t_{PLH}$	1.8	8.8	1.6	9.3	ns
		$t_{PHL}$	5†				
Output Low to High Z		$t_{PLZ}$	5	10.3	1.8	10.8	ns
High Z to Output Low	(05)	$t_{PZL}$	5	8.8	1.6	9.3	ns
Power Dissipation Capacitance	$C_{PD}\S$	—	115 Typ.		115 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

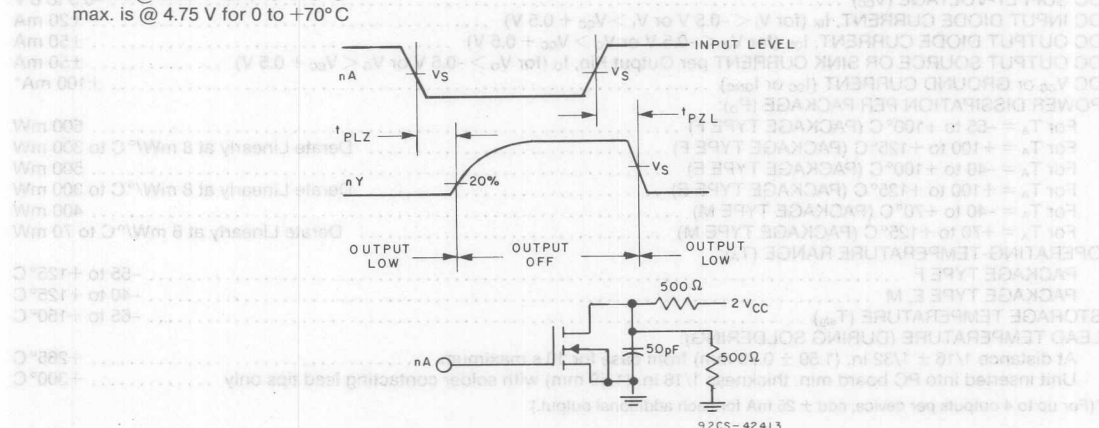
§ $C_{PD}$  is used to determine the dynamic power consumption, per inverter.For AC,  $PD = V_{CC}^2 f_i (C_{PD} + C_L)$ For ACT,  $PD = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ , where  $f_i$  = input frequency $C_L$  = output load capacitance $V_{CC}$  = supply voltage.

Fig. 2 - Propagation delay times and test circuit - AC/ACT05.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$



# CD54/74AC08 CD54/74ACT08

CHARACTERISTIC		SYMBOL	V <sub>CC</sub> (V)	MIN	MAX	TEST CONDITIONS
Propagation Delay Input to Output	(04)	<i>t</i> <sub>PLH</sub>	ns	1.5	1.8	V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C, C <sub>L</sub> = 50 pF
				1.5	1.8	V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C, C <sub>L</sub> = 50 pF
High Z to Output Low	(05)	<i>t</i> <sub>PLZ</sub>	ns	1.5	1.8	V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C, C <sub>L</sub> = 50 pF
				1.5	1.8	V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C, C <sub>L</sub> = 50 pF
Output Low to High Z	(06)	<i>t</i> <sub>PHZ</sub>	ns	1.5	1.8	V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C, C <sub>L</sub> = 50 pF
				1.5	1.8	V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C, C <sub>L</sub> = 50 pF
Power Dissipation Capacitance		C <sub>PD</sub>	pF	100	100	V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C
Input Capacitance		C <sub>i</sub>	pF	10	10	V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C

14

V<sub>CC</sub>

13

4B

12

4A

11

4Y

10

3B

9

3A

8

3Y

7

GND

6

2Y

5

2B

4

2A

3

1Y

2

1B

1

1A

MAX

MIN

0 to +10°C

-40 to +125°C

-55 to +125°C

-55 to +125°C

UNIT

■ Buffered inputs

■ Typical propagation delay (AC08):  
4.3 ns @ V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, C<sub>L</sub> = 50 pF

FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

The GE/RCA-CD54/74AC08 and CD54/74ACT08 are quad 2-input AND gates that utilize GE/RCA's new ADVANCED CMOS LOGIC technology. The CD54AC08 and CD54ACT08 are supplied in 14-lead dual-in-line ceramic packages (F suffix). The CD74AC08 and CD74ACT08 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).

TRUTH TABLE

Inputs		Output
nA	nB	nY
L	L	L
H	L	L
L	H	L
H	H	H

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5 \text{ V}$ or $V_i > V_{CC} + 0.5 \text{ V}$ )	$\pm 20 \text{ mA}$
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5 \text{ V}$ or $V_o > V_{CC} + 0.5 \text{ V}$ )	$\pm 50 \text{ mA}$
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5 \text{ V}$ or $V_o < V_{CC} + 0.5 \text{ V}$ )	$\pm 50 \text{ mA}$
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100 \text{ mA}^*$
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at $8 \text{ mW}/^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at $8 \text{ mW}/^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at $6 \text{ mW}/^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32 \text{ in.}$ ( $1.59 \pm 0.79 \text{ mm}$ ) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16 \text{ in.}$ ( $1.59 \text{ mm}$ ) with solder contacting lead tips only	$+300^\circ\text{C}$

\* (For up to 4 outputs per device; add  $\pm 25 \text{ mA}$  for each additional output.)

Input Level	$V_{CC}$	5.0 V
Input Switching Voltage, $V_i$	$V_{CC}$	5.0 V
Output Switching Voltage, $V_o$	$V_{CC}$	5.0 V

**Technical Data**  
**CD54/74AC08**  
**CD54/74ACT08**

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40 -55	+125 +125	°C °C
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

**STATIC ELECTRICAL CHARACTERISTICS: AC Series**

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# CD54/74AC08 CD54/74ACT08

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin, TTL Inputs High, 1 Unit Load		ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	4.5 to 5.5		2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
All	0.3

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC08 CD54/74ACT08

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	$t_{PLH}$	1.5	—	102	—	109	ns
	$t_{PHL}$	3.3*	2.5	11.3	2.2	12.2	
		5†	1.7	8.1	1.5	8.7	
Power Dissipation Capacitance	$C_{PD}\S$	—	100 Typ.		100 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	$t_{PLH}$	5†	2.6	12.9	2.4	13.8	ns
	$t_{PHL}$						
Power Dissipation Capacitance	$C_{PD}\S$	—	115 Typ.		115 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

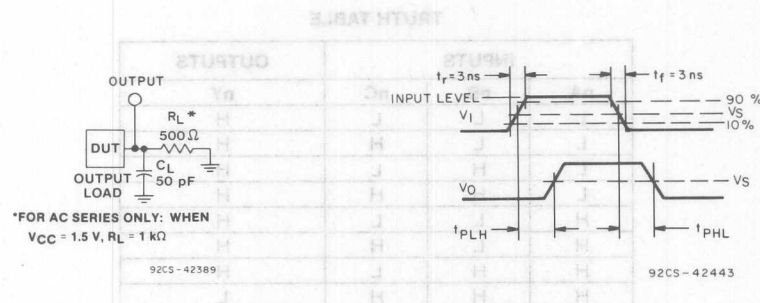
†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

$\S C_{PD}$  is used to determine the dynamic power consumption, per gate.

For AC series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

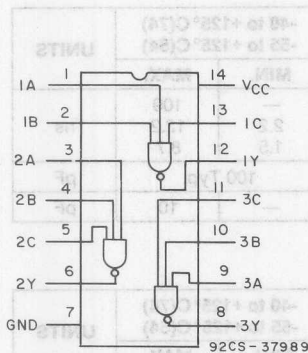


	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_s$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_s$	0.5 $V_{CC}$	0.5 $V_{CC}$

Fig. 1 - Propagation delay times and test circuit.



# CD54/74AC10 CD54/74ACT10



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

The RCA CD54/74AC10 and CD54/74ACT10 are triple 3-input NAND gates that utilize RCA's new ADVANCED CMOS LOGIC technology. The CD54AC10 and CD54ACT10 are supplied in 14-lead dual-in-line ceramic packages (F suffix). The CD74AC10 and CD74ACT10 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).

## Triple 3-Input NAND Gate

### Type Features:

- Typical propagation delay (AC10):  
6 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC type features 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

### TRUTH TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

Input Level	Output Level	Input Switching Voltage $V_{IS}$	Output Switching Voltage $V_{OS}$
$V_{CC}$	$V_{CC}$	0.5 $V_{CC}$	0.5 $V_{CC}$
0.5 $V_{CC}$	0.5 $V_{CC}$	0.5 $V_{CC}$	0.5 $V_{CC}$
0.5 $V_{CC}$	0.5 $V_{CC}$	0.5 $V_{CC}$	0.5 $V_{CC}$

# CD54/74AC10 CD54/74ACT10

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\* (For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A =$ Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_i, V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\* Unless otherwise specified, all voltages are referenced to ground.

# STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS		$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS
						+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
			$V_I$ (V)	$I_O$ (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	$V_{IH}$			1.5 3.0 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V	
Low-Level Input Voltage	$V_{IL}$			1.5 3.0 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V	
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$  # *	-0.05	1.5	1.40	—	1.40	—	1.40	—	V	
			-0.05	3.0	2.90	—	2.90	—	2.90	—		
			-0.05	4.5	4.40	—	4.40	—	4.40	—		
			-4	3.0	2.58	—	2.48	—	2.40	—		
			-24	4.5	3.94	—	3.80	—	3.70	—		
			-75	5.5	—	—	3.85	—	—	—		
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$  # *	0.05	1.5	—	0.10	—	0.10	—	0.10	V	
			0.05	3.0	—	0.10	—	0.10	—	0.10		
			0.05	4.5	—	0.10	—	0.10	—	0.10		
			12	3.0	—	0.36	—	0.44	—	0.50		
			24	4.5	—	0.36	—	0.44	—	0.50		
			75	5.5	—	—	—	1.65	—	—		
Input Leakage Current	$I_I$	$V_{CC}$ or GND		5.5	—	±0.1	—	±1	—	±1	μA	
Quiescent Supply Current, SSI	$I_{CC}$	$V_{CC}$ or GND	0	5.5	—	4	—	40	—	80	μA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# CD54/74AC10

## CD54/74ACT10

### STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS
				+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
	$V_I$ (V)	$I_O$ (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage $V_{IH}$			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage $V_{IL}$			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage $V_{OH}$	$V_{IH}$ or $V_{IL}$ # *	-0.05	4.5	4.40	—	4.40	—	4.40	—	V
		-24	4.5	3.94	—	3.80	—	3.70	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage $V_{OL}$	$V_{IH}$ or $V_{IL}$ # *	0.05	4.5	—	0.10	—	0.10	—	0.10	V
		24	4.5	—	0.36	—	0.44	—	0.50	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current $I_I$	$V_{CC}$ or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI $I_{CC}$	$V_{CC}$ or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load $\Delta I_{CC}$	$V_{CC}-2.1$		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
ALL	

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

INPUT	UNIT LOAD*
ALL	



CD54/74AC10  
CD54/74ACT10

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70° -40 to +85°		-40 to +125(74) -55 to +125(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	$t_{PLH}$ $t_{PHL}$	1.5 3.3* 5†	— 3.3 2.2	137 15.3 10.9	— 3.2 2.1	153 17.1 12.2	ns
Power Dissipation Capacitance	$C_{PD}$ §	—					pF
Input Capacitance	$C_I$	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125(74) -55 to +125(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	$t_{PLH}$ $t_{PHL}$	5†	2.4	12.1	2.3	13.5	ns
Power Dissipation Capacitance	$C_{PD}$ §	—					pF
Input Capacitance	$C_I$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

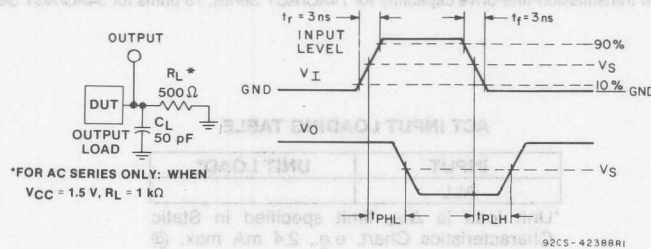
†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§ $C_{PD}$  is used to determine the dynamic power consumption, per gate.

For AC series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

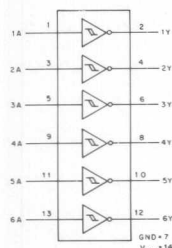
For ACT series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.



	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$

Fig. 1 - Propagation delay times and test circuit.

# CD54/74AC14 CD54/74ACT14

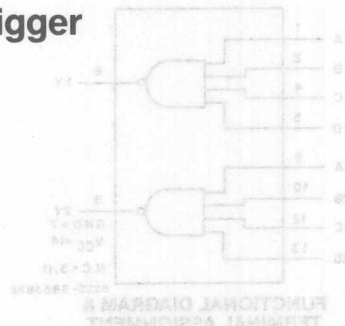


FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

## Hex Inverting Schmitt Trigger

### Type Features:

- Unlimited input rise and fall times
- Exceptionally high noise immunity



The RCA CD54/74AC14 and CD54/74ACT14 each contain six inverting Schmitt Triggers in one package. These devices utilize RCA's new ADVANCED CMOS LOGIC technology.

The CD54AC14 and CD54ACT14 are supplied in 14-lead ceramic dual-in-line packages (F suffix). The CD74AC14 and CD74ACT14 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24$ -mA output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

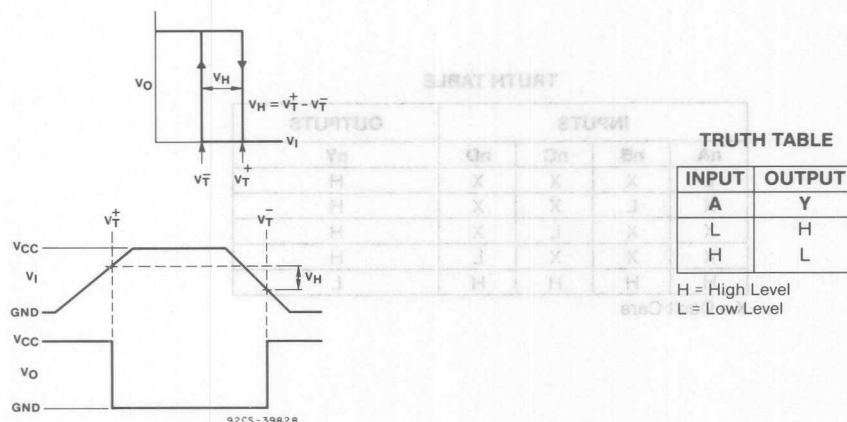
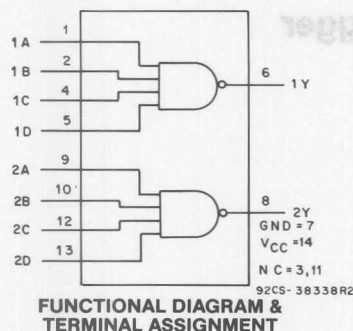


Fig. 1 - Hysteresis definition and characteristic.

# CD54/74AC20 CD54/74ACT20



## Dual 4-Input NAND Gate

### Type Features:

- Typical propagation delay (AC20):  
6 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

The RCA CD54/74AC20 and CD54/74ACT20 are dual 4-input NAND gates that utilize RCA's new ADVANCED CMOS LOGIC technology. The CD54AC20 and CD54ACT20 are supplied in 14-lead dual-in-line ceramic packages (F suffix). The CD74AC20 and CD74ACT20 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS				OUTPUTS
nA	nB	nC	nD	nY
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

X = Don't Care

# CD54/74AC20 CD54/74ACT20

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ OR GROUND CURRENT ( $I_{CC}$ OR $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 $\pm$ 1/32 in. (1.59 $\pm$ 0.79 mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.



# CD54/74AC20

## CD54/74ACT20

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS		$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS
						+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
			$V_I$ (V)	$I_O$ (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	$V_{IH}$			1.5 3.0 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V	
Low-Level Input Voltage	$V_{IL}$			1.5 3.0 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V	
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	1.5	1.40	—	1.40	—	1.40	—	V	
			-0.05	3.0	2.90	—	2.90	—	2.90	—		
			-0.05	4.5	4.40	—	4.40	—	4.40	—		
			-4	3	2.58	—	2.48	—	2.40	—		
			-24	4.5	3.94	—	3.80	—	3.70	—		
			-75	5.5	—	—	3.85	—	—	—		
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$	-50	5.5	—	—	—	—	3.85	—	V	
			0.05	1.5	—	0.10	—	0.10	—	0.10		
			0.05	3.0	—	0.10	—	0.10	—	0.10		
			0.05	4.5	—	0.10	—	0.10	—	0.10		
			12	3.0	—	0.36	—	0.44	—	0.50		
			24	4.5	—	0.36	—	0.44	—	0.50		
Input Leakage Current	$I_I$	$V_{CC}$ or GND	#	75	5.5	—	—	—	1.65	—	$\mu A$	
			*	50	5.5	—	—	—	—	1.65		
Quiescent Supply Current, SSI	$I_{CC}$	$V_{CC}$ or GND	0	5.5	—	4	—	40	—	80	$\mu A$	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# CD54/74AC20 CD54/74ACT20

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS
				+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
	$V_I$ (V)	$I_O$ (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage $V_{IH}$			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage $V_{IL}$			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage $V_{OH}$	$V_{IH}$ or $V_{IL}$ # *	-0.05	4.5	4.40	—	4.40	—	4.40	—	V
		-24	4.5	3.94	—	3.80	—	3.70	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage $V_{OL}$	$V_{IH}$ or $V_{IL}$ # *	0.05	4.5	—	0.10	—	0.10	—	0.10	V
		24	4.5	—	0.36	—	0.44	—	0.50	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current $I_I$	$V_{CC}$ or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI $I_{CC}$	$V_{CC}$ or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load $\Delta I_{CC}$	$V_{CC}-2.1$		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
ALL	0.27

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Output Switching Voltage, $V_o$	Input Switching Voltage, $V_i$	$V_{CC}$
0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>	3 V
0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>	2.5 V
0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>	1.5 V

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70° -40 to +85°		-40 to +125(74) -55 to +125(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	$t_{PLH}$ $t_{PHL}$	1.5 3.3* 5†	— 3.3 2.2	137 15.3 10.9	— 3.2 2.1	153 17.1 12.2	ns
Power Dissipation Capacitance	$C_{PD}$ §	—	—	10	—	10	pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70° C -40 to +85° C		-40 to +125(74) -55 to +125(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	$t_{PLH}$ $t_{PHL}$	5†	2.4	12.1	2.3	13.5	ns
Power Dissipation Capacitance	$C_{PD}$ §	—	—	10	—	10	pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

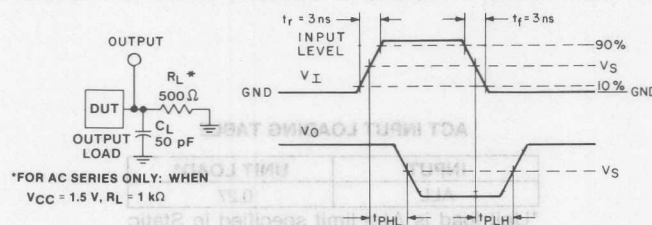
†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70° C  
max. is @ 4.75 V for 0 to +70° C

§ $C_{PD}$  is used to determine the dynamic power consumption, per gate.

For AC series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

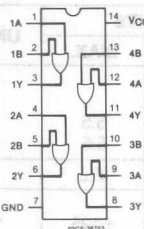


	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$

Fig. 1 - Propagation delay times and test circuit.

# CD54/74AC32

## CD54/74ACT32



**FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT**

The GE/RCA-CD54/74AC32 and CD54/74ACT32 are quad 2-input OR gates that utilize GE/RCA's new ADVANCED CMOS LOGIC technology. The CD54AC32 and CD54ACT32 are supplied in 14-lead dual-in-line ceramic packages (F suffix). The CD74AC32 and CD74ACT32 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).

**TRUTH TABLE**

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

### Quad 2-Input OR Gate

#### Type Features:

- Buffered inputs
- Typical propagation delay:  
4.5 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

#### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

#### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ )	$\pm 20\text{ mA}$
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ )	$\pm 50\text{ mA}$
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5\text{ V}$ or $V_O < V_{CC} + 0.5\text{ V}$ )	$\pm 50\text{ mA}$
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100\text{ mA}$ *

#### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW

#### OPERATING-TEMPERATURE RANGE ( $T_A$ ):

PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$

#### LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79\text{ mm}$ ) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59\text{ mm}$ ) with solder contacting lead tips only	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25\text{ mA}$  for each additional output.)

# CD54/74AC32 CD54/74ACT32

## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}^*$ : (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	
Operating Temperature, $T_A$ :			
CD74 Types	-40	+125	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS
				+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
	$V_I$ (V)	$I_O$ (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage $V_{IH}$			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage $V_{IL}$			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage $V_{OH}$	$V_{IH}$ or $V_{IL}$ # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage $V_{OL}$	$V_{IH}$ or $V_{IL}$ # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current $I_I$	$V_{CC}$ or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI $I_{CC}$	$V_{CC}$ or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.



Technical Data  
**CD54/74AC32**  
**CD54/74ACT32**

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS	
			+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage $V_{IH}$			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage $V_{IL}$			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage $V_{OH}$	$V_{IH}$ or $V_{IL}$ # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage $V_{OL}$	$V_{IH}$ or $V_{IL}$ # *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current $I_I$	$V_{CC}$ or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI $I_{CC}$	$V_{CC}$ or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin, TTL Inputs High, 1 Unit Load $\Delta I_{CC}$	$V_{CC}$ -2.1		4.5 to 5.5		2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
ALL	0.42

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Output Switching Voltage, $V_o$	Input Switching Voltage, $V_i$	Input Level
0.5 V	0.5 V	$V_{CC}$
1.5 V	0.5 V	$V_{CC}$
3 V	0.5 V	$V_{CC}$

# CD54/74AC32 CD54/74ACT32

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	$t_{PLH}$ $t_{PHL}$	1.5 3.3* 5†	— 2.6 1.7	107 11.9 8.5	— 2.4 1.6	119 13.3 9.5	ns
Power Dissipation Capacitance	$C_{PD}\S$	—	47 Typ.		47 Typ.		pF
Input Capacitance	$C_I$	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	$t_{PLH}$ $t_{PHL}$	5†	2.2	10.9	2.1	12.1	ns
Power Dissipation Capacitance	$C_{PD}\S$	—	67 Typ.		67 Typ.		pF
Input Capacitance	$C_I$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

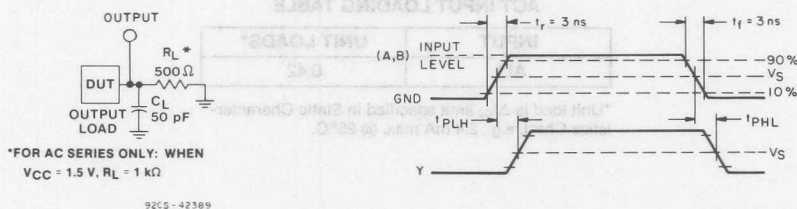
§ $C_{PD}$  is used to determine the dynamic power consumption, per gate.

For AC series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency

$C_L$  = output load capacitance

$V_{CC}$  = supply voltage.



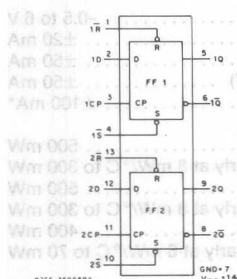
	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$

Fig. 1 - Propagation delay times and test circuit.

## Advance Information

# CD54/74AC74

## CD54/74ACT74



**FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT**

The GE/RCA CD54/74AC74 and CD54/74ACT74 are dual D-type, positive-edge-triggered flip-flops that utilize GE/RCA's new ADVANCED CMOS LOGIC technology. These flip-flops have independent DATA, SET, RESET, and CLOCK inputs and Q and  $\bar{Q}$  outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. SET and RESET are independent of the clock and are accomplished by a low level at the appropriate input.

The CD54AC/ACT74 are supplied in 14-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT74 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).

**Type Features:**

- Buffered inputs
- Typical propagation delay:  
4.9 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

**Family Features:**

- Exceeds 2-kV ESD Protection - MIL-STD 883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

**TRUTH TABLE**

INPUTS				OUTPUTS	
SET	RESET	CP	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	—	H	H	L
H	H	—	L	L	H
H	H	L	X	Q0	$\bar{Q}0$

H = High level (steady state), L = Low level (steady state),  
X = Don't care, — = Transition from Low to High level

NOTES: Q0 = the level of Q before the indicated input conditions were established.

\*This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
<b>POWER DISSIPATION PER PACKAGE (<math>P_D</math>):</b>	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
<b>OPERATING-TEMPERATURE RANGE (<math>T_A</math>):</b>	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
<b>STORAGE TEMPERATURE (<math>T_{stg}</math>)</b>	-65 to $+150^\circ\text{C}$
<b>LEAD TEMPERATURE (DURING SOLDERING):</b>	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ : (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5	5.5	V
	4.5	5.5	V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40	$+125$	$^\circ\text{C}$
	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0	50	ns/V
	0	20	ns/V
	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

# CD54/74AC74

## CD54/74ACT74

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub>	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
		or	-0.05	4.5	4.4	—	4.4	—	4.4	—	
		V <sub>IL</sub>	-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
		#	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	3.85	—		
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub>	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
		or	0.05	4.5	—	0.1	—	0.1	—	0.1	
		V <sub>IL</sub>	12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
		#	75	5.5	—	—	1.65	—	—	—	
		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
Quiescent Supply Current, FF	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.



# CD54/74AC74 CD54/74ACT74

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS	
				+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)			
	$V_I$ (V)	$I_O$ (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	$V_{IH}$	—	4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	$V_{IL}$	—	4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		#	-24	4.5	3.94	—	3.8	—	3.7	—	
		#	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	3.85	—		
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.05	4.5	—	±0.1	—	±1	—	±1	V
		#	24	4.5	—	0.36	—	0.44	—	0.5	
		#	75	5.5	—	—	—	1.65	—	—	
		*	50	5.5	—	—	—	—	1.65		
Input Leakage Current	$I_I$	$V_{CC}$ or GND	5.5	—	±0.1	—	±1	—	±1	μA	
Quiescent Supply Current, FF	$I_{CC}$	$V_{CC}$ or GND	5.5	—	4	—	40	—	80	μA	
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	$\Delta I_{CC}$	$V_{CC}-2.1$	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
D	0.53
$\bar{R}, \bar{S}$	0.58
CP	1

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC74 CD54/74ACT74

## PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t <sub>SU</sub>	1.5 3.3* 5†	68 9.5 5.5	—	76 10.7 6.1	—	ns
Hold Time	t <sub>H</sub>	1.5 3.3 5	0 0 0	—	0 0 0	—	ns
Removal Time R, S to CP	t <sub>REM</sub>	1.5 3.3 5	30 4.2 2.4	—	34 4.7 2.7	—	ns
Pulse Width R, S	t <sub>W</sub>	1.5 3.3 5	64 9 5.1	—	73 10.2 5.8	—	ns
Pulse Width CP	t <sub>W</sub>	1.5 3.3 5	63 9 5	—	72 10 5.7	—	ns
CP Frequency	f <sub>MAX</sub>	1.5 3.3 5	8 56 100	—	7 50 88	—	MHz

\*3.3 V: min. is @ 3 V  
†5 V: min. is @ 4.5 V  
5 V: min is @ 4.75 V for 0 to +70°C

## SWITCHING CHARACTERISTICS: AC Series, t<sub>r</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q, $\bar{Q}$	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3* 5†	— 3.1 2	118 13.2 9.4	— 3 1.9	132 14.7 10.5	ns
$\bar{R}, \bar{S}$ to Q, $\bar{Q}$	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 3.1 2	118 13.2 9.4	— 3 1.9	132 14.7 10.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	86 Typ.		86 Typ.		pF
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V  
†5 V: min. is @ 5.5 V  
max. is @ 4.5 V  
5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per flip-flop.  
PD = C<sub>PD</sub>V<sub>CC</sub><sup>2</sup> f<sub>i</sub> + Σ (C<sub>L</sub> V<sub>CC</sub><sup>2</sup> f<sub>o</sub>) where f<sub>i</sub> = input frequency  
f<sub>o</sub> = output frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.

Output Switching Voltage, V <sub>o</sub>	0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>
Input Switching Voltage, V <sub>i</sub>	0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>
Input Level	V <sub>CC</sub>	3 V

# CD54/74AC74 CD54/74ACT74

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t <sub>SU</sub>	5*	6.5	—	7.3	—	ns
Hold Time	t <sub>H</sub>	5	0	—	0	—	ns
Removal Time R, S to CP	t <sub>REM</sub>	5	3	—	3.4	—	ns
Pulse Width R, S	t <sub>w</sub>	5	5.1	—	5.8	—	ns
Pulse Width CP	t <sub>w</sub>	5	5.6	—	6.3	—	ns
CP Frequency	f <sub>MAX</sub>	5	90	—	80	—	MHz

\*Min. is @ 4.5 V

Min. is @ 4.75 V for 0 to +70°C

SWITCHING CHARACTERISTICS: ACT Series, t<sub>r</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q, Q̄	t <sub>PLH</sub> t <sub>PHL</sub>	5*	—	9.4	—	10.5	ns
R, S to Q, Q̄	t <sub>PLH</sub> t <sub>PHL</sub>	5	—	9.4	—	10.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> †	—	86 Typ.		86 Typ.		pF
Input Capacitance	C <sub>I</sub>	—	—	10	10	—	pF

\*Min. is @ 5.5 V

Max. is @ 4.5 V.

Min. is @ 5.25 V for 0 to +70°C

Max. is @ 4.75 V for 0 to +70°C

†C<sub>PD</sub> is used to determine the dynamic power consumption, per flip-flop.

PD = C<sub>PD</sub>V<sub>CC</sub><sup>2</sup>f<sub>i</sub> + Σ(C<sub>L</sub>V<sub>CC</sub><sup>2</sup>f<sub>o</sub>) + V<sub>CC</sub>ΔI<sub>CC</sub> where f<sub>i</sub> = input frequency

f<sub>o</sub> = output frequency

C<sub>L</sub> = output load capacitance

V<sub>CC</sub> = supply voltage.

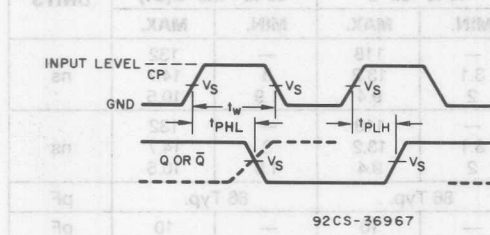


Fig. 1 - Clock prerequisite and propagation delays.

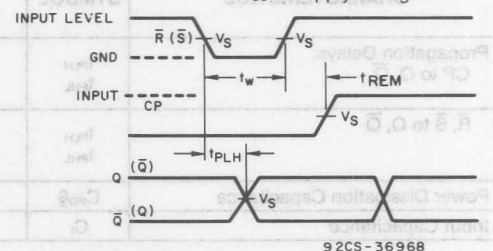


Fig. 2 - Reset or Set prerequisite and propagation delays.

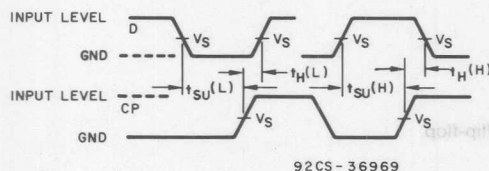
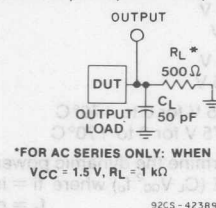


Fig. 3 - Data prerequisite times.



\*FOR AC SERIES ONLY: WHEN  
V<sub>CC</sub> = 1.5 V, R<sub>L</sub> = 1 kΩ

	CD54/74AC	CD54/74ACT
Input Level	V <sub>CC</sub>	3 V
Input Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	1.5 V
Output Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>

## Advance Information

# CD54/74AC86

## CD54/74ACT86

### Quad 2-Input Exclusive-OR Gate

## Type Features:

- Buffered inputs
- Typical propagation delay:  
5.1 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

#### FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

The GE/RCA-CD54/74AC86 and CD54/74ACT86 are quad 2-input Exclusive-OR gates that utilize GE/RCA's new ADVANCED CMOS LOGIC technology. The CD54AC86 and CD54ACT86 are supplied in 14-lead dual-in-line ceramic packages (F suffix). The CD74AC86 and CD74ACT86 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).

#### TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
H	H	L
H	L	H
L	H	H

## Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

#### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ )	$\pm 20\text{ mA}$
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ )	$\pm 50\text{ mA}$
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5\text{ V}$ or $V_O < V_{CC} + 0.5\text{ V}$ )	$\pm 50\text{ mA}$
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100\text{ mA}$ *

#### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at $8\text{ mW}/^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at $8\text{ mW}/^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at $6\text{ mW}/^\circ\text{C}$ to 70 mW

#### OPERATING-TEMPERATURE RANGE ( $T_A$ ):

PACKAGE TYPE F	$-55$ to $+125^\circ\text{C}$
PACKAGE TYPE E, M	$-40$ to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	$-65$ to $+150^\circ\text{C}$

#### LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79\text{ mm}$ ) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59\text{ mm}$ ) with solder contacting lead tips only	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25\text{ mA}$  for each additional output.)

# RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}^*$ : (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40 -55	+125 +125	°C °C
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
	V <sub>i</sub> (V)	I <sub>o</sub> (mA)		+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I <sub>i</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.



# CD54/74AC86 CD54/74ACT86

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS
					+25		0 to +70		-40 to +125(74)		
							-40 to +85		-55 to +125(54)		
		$V_I$ (V)	$I_O$ (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	$V_{IH}$			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	$V_{IL}$			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
		#	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	3.85	—	—	
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
		#	75	5.5	—	—	—	1.65	—	—	
		*	50	5.5	—	—	—	—	1.65	—	
Input Leakage Current	$I_I$	$V_{CC}$ or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI	$I_{CC}$	$V_{CC}$ or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	$\Delta I_{CC}$	$V_{CC}$ -2.1		4.5 to 5.5		2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
ALL	0.48

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC	CD54/74ACT
3 V	$V_{CC}$
1.5 V	0.5 $V_{CC}$
0.5 V	0.5 $V_{CC}$

Fig. 1 - Propagation delay times and test circuit.

# CD54/74AC86 CD54/74ACT86

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Outputs	$t_{PLH}$	1.5	—	119	—	135	ns
	$t_{PHL}$	3.3*	2.9	13.6	2.8	15.1	
		5†	1.9	9.7	1.8	10.8	
Power Dissipation Capacitance	$C_{PD}\S$	—	57 Typ.		57 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Outputs	$t_{PLH}$	5†	2.6	13	2.5	14.6	ns
	$t_{PHL}$						
Power Dissipation Capacitance	$C_{PD}\S$	—	81 Typ.		81 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

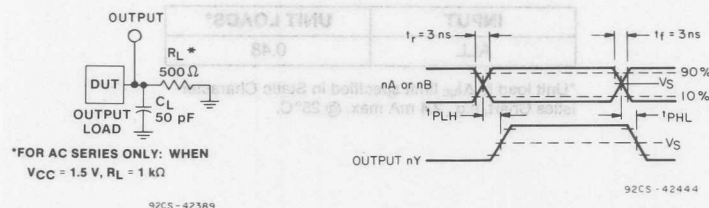
†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§ $C_{PD}$  is used to determine the dynamic power consumption, per gate.

For AC series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

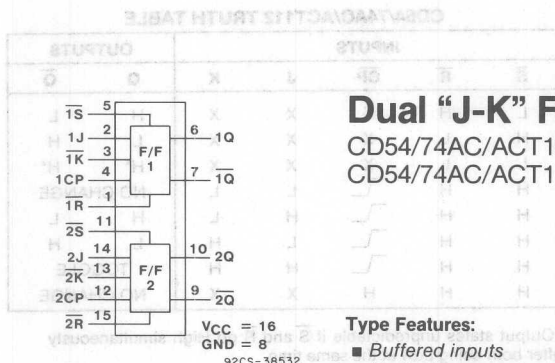
For ACT series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.



\*FOR AC SERIES ONLY: WHEN  
 $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$

Fig. 1 - Propagation delay times and test circuit.



CD54/74ACT109  
FUNCTIONAL DIAGRAM

## Dual "J-K" Flip-Flop with Set and Reset

CD54/74AC/ACT109 - Positive-Edge-Triggered (J,  $\bar{K}$ )  
CD54/74AC/ACT112 - Negative-Edge-Triggered (J, K)

### Type Features:

- Buffered inputs
- Typical propagation delay:  
4.8 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

The RCA CD54/74AC109, -112 and CD54/74ACT109, -112 are dual "J-K" flip-flops with set and reset that utilize RCA's new ADVANCED CMOS LOGIC technology. These flip-flops have independent J, K (or  $\bar{K}$ ), Set, Reset, and Clock inputs and Q and  $\bar{Q}$  outputs. The CD54/74ACT112 changes state on the negative-going transition of the clock pulse. The CD54/74AC/ACT109 changes state on the positive-going transition of the clock. Set and Reset are accomplished asynchronously by low-level inputs.

The CD54AC/ACT109 and CD54AC/ACT112 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT109 and CD74AC/ACT112 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

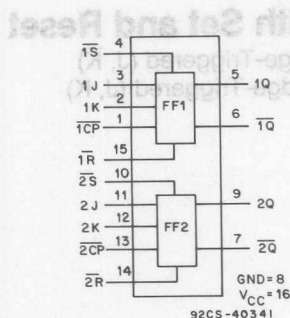
CD54/74AC/ACT109 TRUTH TABLE

INPUTS					OUTPUTS	
$\bar{S}$	$\bar{R}$	CP	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H		L	L	L	H
H	H		H	L	TOGGLE	
H	H		L	H	NO CHANGE	
H	H		H	H	L	L
H	H	L	X	X	NO CHANGE	

\*Unpredictable and unstable condition if both  $\bar{S}$  and  $\bar{R}$  go high simultaneously.

UNITS	LIMITS		
	MAX	MIN	
V	5.5	1.5	Supply Voltage Range, V <sub>CC</sub>
V	5.5	0	DC Input or Output Voltage, V <sub>I</sub> , V <sub>O</sub>
V	V <sub>CC</sub>	0	Operating Voltage, V <sub>CC</sub>
°C	+125	-55	Operating Temperature, T <sub>A</sub>
ns	50	0	Input Rise and Fall Time, t <sub>r</sub> , t <sub>f</sub>
ns	50	0	at 1.5 V to 5 V (AC Types)
ns	50	0	at 2.5 V to 5 V (AC Types)
ns	10	0	at 4.5 V to 5.5 V (ACT Types)

# CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112



CD54/74AC/ACT112  
FUNCTIONAL DIAGRAM

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	.....	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	.....	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	.....	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	.....	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	.....	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):		
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	.....	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	.....	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	.....	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	.....	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	.....	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	.....	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):		
PACKAGE TYPE F	.....	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	.....	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	.....	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	.....	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	.....	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *, (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	+125	$^\circ\text{C}$
CD54 Types	-55	+125	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

CD54/74AC/ACT112 TRUTH TABLE

INPUTS					OUTPUTS	
$\bar{S}$	$\bar{R}$	$\bar{CP}$	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
L	H		L	L	NO CHANGE	
H	H		H	L	H	L
H	H		L	H	L	H
H	H		H	H	TOGGLE	
H	H	H	X	X	NO CHANGE	

\*Output states unpredictable if  $\bar{S}$  and  $\bar{R}$  go High simultaneously after both being Low at the same time.

H = High steady state

L = Low steady state

X = Irrelevant

= High-to-Low transition

= Low-to-High transition

# CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112

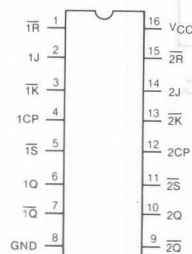
## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V
Low-Level Input Voltage	V <sub>IL</sub>			1.5 3 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-50	5.5	—	—	—	—	3.85	—	V
			0.05	1.5	—	0.1	—	0.1	—	0.1	
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	75	5.5	—	—	—	1.65	—	—	μA
			50	5.5	—	—	—	—	—	—	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

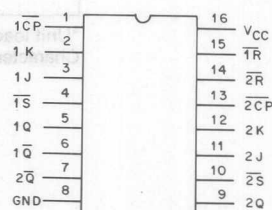
\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

## TERMINAL ASSIGNMENT DIAGRAMS



92CS-36761

CD54/74AC/ACT109



92CS-40339

CD54/74AC/ACT112



STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	4.5	—	0.10	—	0.10	—	0.10	V
			24	4.5	—	0.36	—	0.44	—	0.50	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*	
	109	112
J, CP, $\overline{CP}$	1	1
K	—	0.53
$\overline{K}$	0.53	—
$\overline{S}$ , $\overline{R}$	0.58	0.58

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC109, CD54/74AC112

## CD54/74ACT109, CD54/74ACT112

## PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Maximum CP, ( $\overline{\text{CP}}$ ) Frequency 109	$f_{\text{max}}$	1.5 3.3* 5†		—		—	MHz
112	$f_{\text{max}}$	1.5 3.3 5		—		—	MHz
CP ( $\overline{\text{CP}}$ ) Pulse Width	$t_w$	1.5 3.3 5		—		—	ns
Setup Time J, K to CP 109	$t_{\text{su}}$	1.5 3.3 5		—		—	ns
J, K to $\overline{\text{CP}}$ 112	$t_{\text{su}}$	1.5 3.3 5		—		—	ns
Hold Time J, K to CP 109	$t_{\text{H}}$	1.5 3.3 5		—		—	ns
J, K to $\overline{\text{CP}}$ 112	$t_{\text{H}}$	1.5 3.3 5		—		—	ns
Removal Time R, S to CP ( $\overline{\text{CP}}$ )	$t_{\text{REM}}$	1.5 3.3 5		—		—	ns

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

5 V: min. is @ 4.75 V for 0 to +70°C

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3$  ns,  $C_L = 50$  pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP ( $\overline{\text{CP}}$ ) to Q, $\overline{\text{Q}}$	$t_{\text{PLH}}$ $t_{\text{PHL}}$	1.5 3.3* 5†	— 2.8 1.8	115 12.9 9.2	— 2.7 1.7	129 14.4 10.3	ns
$\overline{\text{S}}, \overline{\text{R}}$ to Q, $\overline{\text{Q}}$	$t_{\text{PLH}}$ $t_{\text{PHL}}$	1.5 3.3 5	— 3.3 2.2	137 15.3 10.9	— 3.2 2.1	153 17.1 12.2	ns
Power Dissipation Capacitance	$C_{\text{PD}}§$	—					pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V†5 V: min. is @ 5.5 V  
max. is @ 4.5 V5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C§ $C_{\text{PD}}$  is used to determine the dynamic power consumption, per flip-flop. $P_D = C_{\text{PD}}V_{\text{CC}}^2 f_i + \Sigma (C_L V_{\text{CC}}^2 f_o)$  where  $f_i$  = input frequency $f_o$  = output frequency $C_L$  = output load capacitance $V_{\text{CC}}$  = supply voltage.

CD54/74AC109, CD54/74AC112  
CD54/74ACT109, CD54/74ACT112

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C (74) -55 to +125°C (54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Maximum CP ( $\overline{\text{CP}}$ ) Frequency 109 112	$f_{\text{max}}$	5*		—		—	MHz
CP ( $\overline{\text{CP}}$ ) Pulse Width	$t_w$	5		—		—	ns
Setup Time J, K to CP (109) J, K to $\overline{\text{CP}}$ (112)	$t_{\text{su}}$	5		—		—	ns
Hold Time J, K to CP (109) J, K to $\overline{\text{CP}}$ (112)	$t_{\text{h}}$	5		—		—	ns
Removal Time R, S to CP ( $\overline{\text{CP}}$ )	$t_{\text{rem}}$	5		—		—	ns

\*min. is @ 4.5 V  
min. is @ 4.75 V for 0 to +70°C

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C (74) -55 to +125°C (54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays CP ( $\overline{\text{CP}}$ ) to Q, $\overline{\text{Q}}$	$t_{\text{PLH}}$	5*	1.8	9.2	1.7	10.3	ns
$\overline{\text{S}}, \overline{\text{R}}$ , to Q, $\overline{\text{Q}}$	$t_{\text{PHL}}$	5	2.4	12.1	2.3	13.5	ns
Power Dissipation Capacitance	$C_{\text{PD}}\S$	—					pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*Min. is @ 5.5 V  
Max. is @ 4.5 V

Min. is @ 5.25 V for 0 to +70°C  
Max. is @ 4.75 V for 0 to +70°C

$\S C_{\text{PD}}$  is used to determine the dynamic power consumption, per flip-flop.

$$P_D = C_{\text{PD}} V_{\text{CC}}^2 f_i + \sum (C_L V_{\text{CC}}^2 f_o) + V_{\text{CC}} \Delta I_{\text{CC}} \text{ where } f_i = \text{input frequency}$$
$$f_o = \text{output frequency}$$
$$C_L = \text{output load capacitance}$$
$$V_{\text{CC}} = \text{supply voltage.}$$

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C (74) -55 to +125°C (54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays CP ( $\overline{\text{CP}}$ ) to Q, $\overline{\text{Q}}$	$t_{\text{PLH}}$	5*	1.8	9.2	1.7	10.3	ns
$\overline{\text{S}}, \overline{\text{R}}$ , to Q, $\overline{\text{Q}}$	$t_{\text{PHL}}$	5	2.4	12.1	2.3	13.5	ns
Power Dissipation Capacitance	$C_{\text{PD}}\S$	—					pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*Min. is @ 5.5 V  
max. is @ 4.5 V

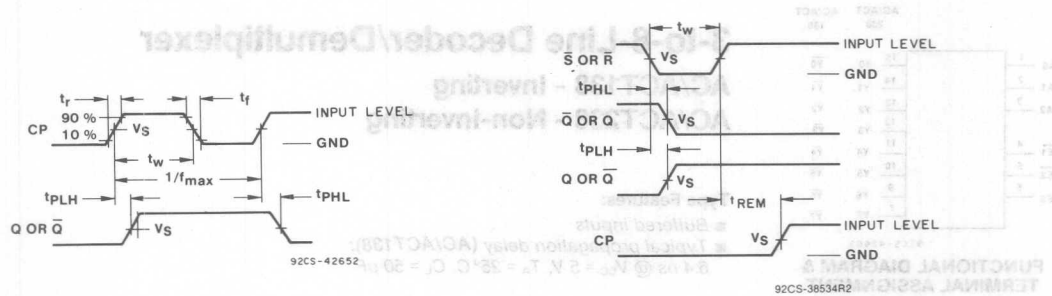
Min. is @ 5.25 V  
max. is @ 4.75 V

Min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

$\S C_{\text{PD}}$  is used to determine the dynamic power consumption, per flip-flop.  
 $P_D = C_{\text{PD}} V_{\text{CC}}^2 f_i + \sum (C_L V_{\text{CC}}^2 f_o) + V_{\text{CC}} \Delta I_{\text{CC}}$  where  $f_i$  = input frequency  
 $f_o$  = output frequency  
 $C_L$  = output load capacitance  
 $V_{\text{CC}}$  = supply voltage.

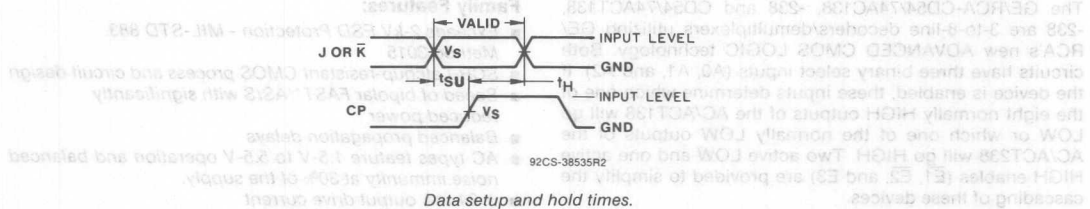
# CD54/74AC109, CD54/74AC112 CD54/74ACT109, CD54/74ACT112

## CD54/74AC/ACT109 Waveforms



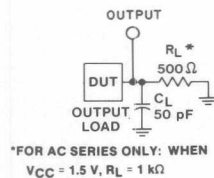
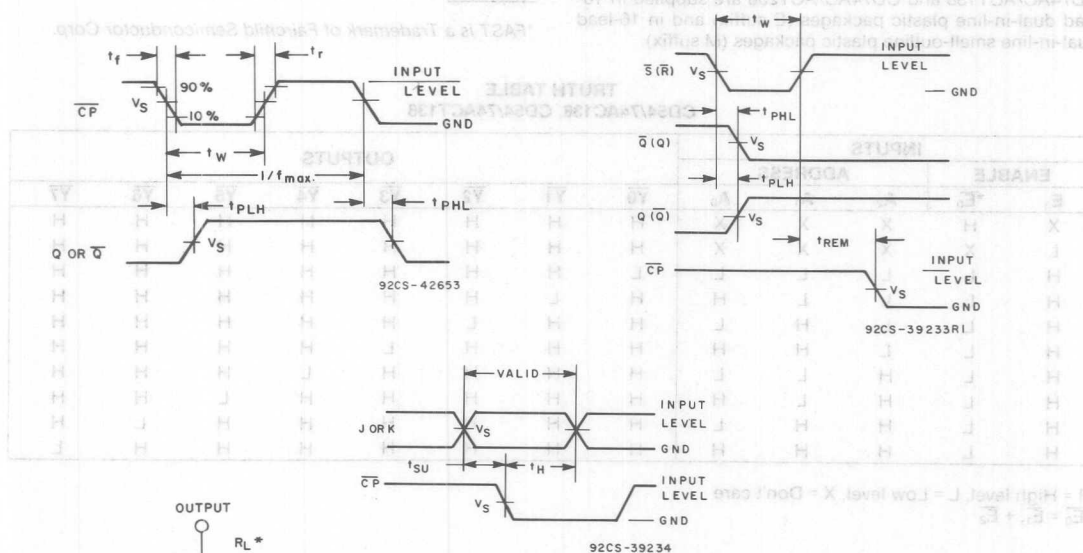
Clock to output delays and clock pulse width.

Reset or Set prerequisite and propagation delays.



Data setup and hold times.

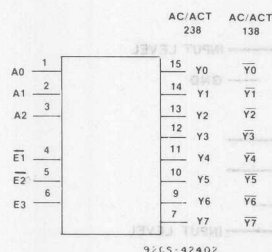
## CD54/74/AC/ACT112 Waveforms



Test circuit.

Propagation delay times, and setup and hold times.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

## 3-to-8-Line Decoder/Demultiplexer

AC/ACT138 - Inverting

AC/ACT238 - Non-Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay (AC/ACT138): 6.4 ns @  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50 pF$

The GE/RCA-CD54/74ACT138, -238 and CD54/74ACT138, -238 are 3-to-8-line decoders/demultiplexers utilizing GE/RCA's new ADVANCED CMOS LOGIC technology. Both circuits have three binary select inputs ( $A_0$ ,  $A_1$ , and  $A_2$ ). If the device is enabled, these inputs determine which one of the eight normally HIGH outputs of the AC/ACT138 will go LOW or which one of the normally LOW outputs of the AC/ACT238 will go HIGH. Two active LOW and one active HIGH enables ( $\overline{E_1}$ ,  $\overline{E_2}$ , and  $E_3$ ) are provided to simplify the cascading of these devices.

The CD54AC/ACT138 and CD54AC/ACT238 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT138 and CD74AC/ACT238 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD 883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- $\pm 24$ -mA output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

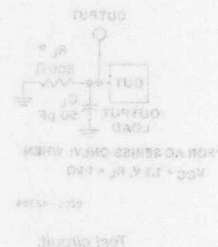
TRUTH TABLE  
CD54/74ACT138, CD54/74ACT238

ENABLE		INPUTS			OUTPUTS							
$E_3$	$\overline{E_0}$	$A_2$	$A_1$	$A_0$	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H = High level, L = Low level, X = Don't care

\* $\overline{E_0} = \overline{E_1} + \overline{E_2}$

CD54/74ACT138	CD54/74ACT238	CD54/74ACT138
3 V	$V_{CC}$	Input Level
1.8 V	0.8 $V_{CC}$	Input Switching Voltage, $V_i$
0.5 $V_{CC}$	0.5 $V_{CC}$	Output Switching Voltage, $V_o$



File Number 1909



# CD54/74AC138, CD54/74AC238

## CD54/74ACT138, CD54/74ACT238

TRUTH TABLE  
CD54/74AC238, CD54/74ACT238

INPUTS					OUTPUTS							
ENABLE		ADDRESS										
E <sub>3</sub>	*E <sub>0</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Y <sub>0</sub>	Y <sub>1</sub>	Y <sub>2</sub>	Y <sub>3</sub>	Y <sub>4</sub>	Y <sub>5</sub>	Y <sub>6</sub>	Y <sub>7</sub>
X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	H	H	L	L	L	H	L	L	L	L
H	L	H	L	L	L	L	L	H	L	L	L	L
H	L	H	L	H	L	L	L	L	H	L	L	L
H	L	H	H	L	L	L	L	L	L	H	L	L
H	L	H	H	H	L	L	L	L	L	L	H	L

H = High level, L = Low level, X = Don't care

\*E<sub>0</sub> = E<sub>1</sub>, + E<sub>2</sub>

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ ) ..... -0.5 to 6 V  
 DC INPUT DIODE CURRENT,  $I_{IK}$  (for  $V_I < -0.5$  V or  $V_I > V_{CC} + 0.5$  V) .....  $\pm 20$  mA  
 DC OUTPUT DIODE CURRENT,  $I_{OK}$  (for  $V_O < -0.5$  V or  $V_O > V_{CC} + 0.5$  V) .....  $\pm 50$  mA  
 DC OUTPUT SOURCE OR SINK CURRENT per Output Pin,  $I_O$  (for  $V_O > -0.5$  V or  $V_O < V_{CC} + 0.5$  V) .....  $\pm 50$  mA  
 DC  $V_{CC}$  or GROUND CURRENT ( $I_{CC}$  or  $I_{GND}$ ) .....  $\pm 100$  mA\*

### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55$  to  $+100^\circ\text{C}$  (PACKAGE TYPE F) ..... 500 mW  
 For  $T_A = +100$  to  $+125^\circ\text{C}$  (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/ $^\circ\text{C}$  to 300 mW  
 For  $T_A = -40$  to  $+100^\circ\text{C}$  (PACKAGE TYPE E) ..... 500 mW  
 For  $T_A = +100$  to  $+125^\circ\text{C}$  (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/ $^\circ\text{C}$  to 300 mW  
 For  $T_A = -40$  to  $+70^\circ\text{C}$  (PACKAGE TYPE M) ..... 400 mW  
 For  $T_A = +70$  to  $+125^\circ\text{C}$  (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/ $^\circ\text{C}$  to 70 mW

### OPERATING-TEMPERATURE RANGE ( $T_A$ ):

PACKAGE TYPE F ..... -55 to  $+125^\circ\text{C}$   
 PACKAGE TYPE E, M ..... -40 to  $+125^\circ\text{C}$

### STORAGE TEMPERATURE ( $T_{stg}$ )

..... -65 to  $+150^\circ\text{C}$

### LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  in. ( $1.59 \pm 0.79$  mm) from case for 10 s maximum .....  $+265^\circ\text{C}$

Unit inserted into PC board min. thickness  $1/16$  in. ( $1.59$  mm) with solder contacting lead tips only .....  $+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

### RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40 -55	+125 +125	$^\circ\text{C}$ $^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

# CD54/74AC138, CD54/74AC238 CD54/74ACT138, CD54/74ACT238

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	1.65	—	—	—	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

CHARACTERISTIC	LIMITS	
	MIN.	MAX.
Supply Voltage Range, $V_{CC}$ (for $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5	5.5
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$
Operating Temperature, $T_A$ CD54 Types CD74 Types	-55	+125
Input Rise and Fall Rate, $dV/dt$ at 1.5 V to 3 V (AC Types) at 3.5 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0	50

# CD54/74AC138, CD54/74AC238 CD54/74ACT138, CD54/74ACT238

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
	V <sub>I</sub> (V)	I <sub>O</sub> (mA)		+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
A0 - A2	0.83
$\bar{E}1, \bar{E}2$	1
E3	0.42

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

# **CD54/74AC138, CD54/74AC238** **CD54/74ACT138, CD54/74ACT238**

**SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$** 

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: An to Output	(138) $t_{PLH}$ $t_{PHL}$	1.5 3.3* 5†	— 4 2.5	152 17.1 12.2	— 3.8 2.4	170 19 13.6	ns
$\overline{E1}, \overline{E2}$ to Output	(138) $t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 3.5 2.5	134 15 10.7	— 3.4 2.1	149 16.7 11.9	ns
E3 to Output	(138) $t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 3.9 2.5	147 16.5 11.8	— 3.7 2.4	165 18.5 13.2	ns
An to Output	(238) $t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 4.4 2.8	168 18.8 13.4	— 4.2 2.7	187 21 15	ns
$\overline{E1}, \overline{E2}$ to Output	(238) $t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 3.9 2.2	150 15 10.7	— 3.8 2.1	167 16.7 11.9	ns
E3 to Output	(238) $t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 4.9 3.1	186 20.9 14.9	— 4.7 3	208 23.2 16.6	ns
Power Dissipation Capacitance	$C_{PD}\ddagger$	—	110 Typ.		110 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

**SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$** 

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: An to Output	(138) $t_{PLH}$ $t_{PHL}$	5†	2.9	13.8	2.7	15.4	ns
$\overline{E1}, \overline{E2}$ to Output	(138) $t_{PLH}$ $t_{PHL}$	5	2.3	10.9	2.2	12.2	ns
E3 to Output	(138) $t_{PLH}$ $t_{PHL}$	5	2.5	12.2	2.4	13.6	ns
An to Output	(238) $t_{PLH}$ $t_{PHL}$	5	2.9	14	2.8	15.6	ns
$\overline{E1}, \overline{E2}$ to Output	(238) $t_{PLH}$ $t_{PHL}$	5	2.6	12.7	2.5	14.2	ns
E3 to Output	(238) $t_{PLH}$ $t_{PHL}$	5	2.5	12.2	2.4	13.6	ns
Power Dissipation Capacitance	$C_{PD}\ddagger$	—	160 Typ.		160 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

‡ $C_{PD}$  is used to determine the dynamic power consumption, per package.

For AC series:  $PD = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT series:  $PD = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

# CD54/74AC138, CD54/74AC238 CD54/74ACT138, CD54/74ACT238

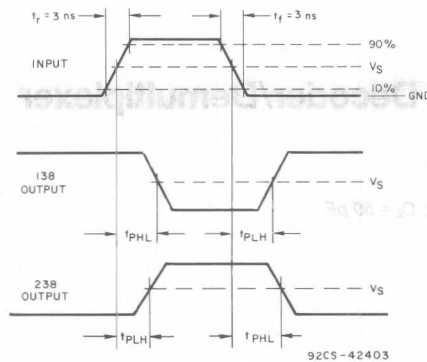


Fig. 1 - Propagation delay times.

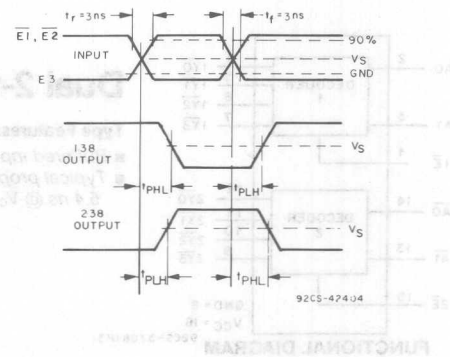


Fig. 2 - Propagation delay times.

	CD54/74AC	CD54/74ACT
Input Level	V <sub>CC</sub>	3 V
Input Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	1.5 V
Output Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>

OUTPUTS				INPUTS		Enable
Y <sub>0</sub>	Y <sub>1</sub>	Y <sub>2</sub>	Y <sub>3</sub>	A <sub>1</sub>	A <sub>0</sub>	
L	H	H	H	L	L	L
H	L	H	H	L	H	L
H	H	L	H	L	L	L
H	H	H	L	L	H	L
H	H	H	H	L	L	L
H	H	H	H	L	H	L
H	H	H	H	L	L	L

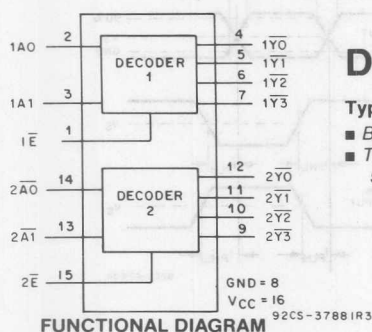
X = Don't care



# CD54/74AC139

## CD54/74ACT139

Advance Information



### Dual 2-to-4-Line Decoder/Demultiplexer

#### Type Features:

- Buffered inputs
- Typical propagation delay:  
5.4 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

The RCA CD54/74AC139 and CD54/74ACT139 are dual 2-to-4-line decoder/demultiplexers that utilize RCA's new ADVANCED CMOS LOGIC technology. These devices contain two independent binary to one-of-four decoders, each with a single active-LOW enable input ( $\overline{1E}$  or  $\overline{2E}$ ). Data on the select inputs (1A0 and 1A1 or 2A0 and 2A1) cause one of the four normally HIGH outputs to go LOW.

If the enable input is HIGH, all four outputs remain HIGH. For demultiplexer operation, the enable input is the data input. The enable input also functions as a chip select when these devices are cascaded.

The CD54AC139 and CD54ACT139 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC139 and CD74ACT139 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline packages (M suffix).

#### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS			OUTPUTS			
Enable	Select					
$\overline{E}$	A1	A0	$\overline{Y3}$	$\overline{Y2}$	$\overline{Y1}$	$\overline{Y0}$
L	L	L	H	H	H	L
L	L	H	H	H	L	H
L	H	L	H	L	H	H
L	H	H	L	H	H	H
H	X	X	H	H	H	H

X = Don't care

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

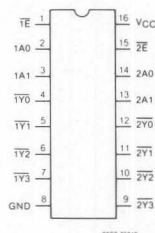
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *, (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

**TERMINAL ASSIGNMENT**

# STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub>	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
		or V <sub>IL</sub>	-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
		#	-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub>	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
		or V <sub>IL</sub>	0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
		#	24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.



TERMINAL ASSIGNMENT

# CD54/74AC139 CD54/74ACT139

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS			$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS
			+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)				
	$V_I$ (V)	$I_O$ (mA)	MIN.		MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	$V_{IH}$		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	$V_{IL}$		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		#	-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		#	24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	$I_i$	$V_{CC}$ or GND	5.5	—	±0.1	—	±1	—	±1	μA	
Quiescent Supply Current, MSI	$I_{CC}$	$V_{CC}$ or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin, TTL Inputs High, 1 Unit Load	$\Delta I_{CC}$	$V_{CC}-2.1$	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

## ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
A0, A1	1
$\bar{E}$	0.67

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

Output Switching Voltage, $V_o$	Input Switching Voltage, $V_i$
0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>
1.5 V	0.8 V <sub>CC</sub>
3 V	V <sub>CC</sub>

# CD54/74AC139 CD54/74ACT139

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: A0, A1 to Outputs	$t_{PLH}$	1.5	—	129	—	144	ns
	$t_{PHL}$	3.3*	3.1	14.2	2.9	16.1	
$\bar{E}$ to Outputs	$t_{PLH}$	5†	2.1	10.3	1.9	11.5	ns
	$t_{PHL}$	5	2.9	13.4	2.7	15	
Power Dissipation Capacitance	$C_{PD}\S$	—	83 Typ.		83 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: A0, A1 to Outputs	$t_{PLH}$	5†	2.7	13.2	2.5	14.7	ns
	$t_{PHL}$	5	2.7	13.2	2.5	14.7	
Power Dissipation Capacitance	$C_{PD}\S$	—	126 Typ.		126 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

$\S C_{PD}$  is used to determine the dynamic power consumption, per decoder/demultiplexer.

For AC series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

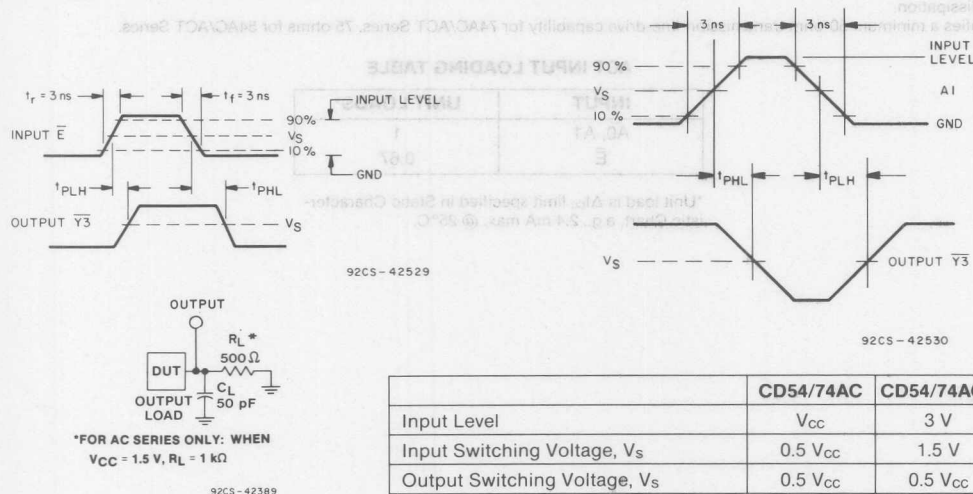


Fig. 1 - Propagation delay times and test circuit.

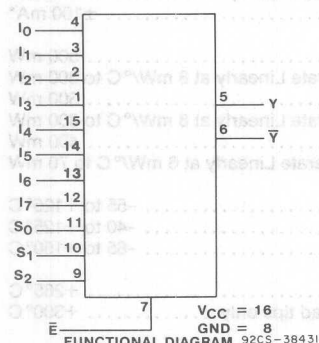


## Advance Information

# CD54/74AC151

## CD54/74ACT151

### 8-Input Multiplexer



## Type Features:

- Buffered inputs
- Typical propagation delay:  
6 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

The RCA CD54/74AC151 and CD54/74ACT151 are 8-input digital multiplexers that utilize RCA's new ADVANCED CMOS LOGIC technology. They have three binary control inputs ( $S_0$ ,  $S_1$ , and  $S_2$ ) and an active-LOW Enable ( $\bar{E}$ ) input. The three binary inputs select 1 of 8 channels. The output is both inverting ( $\bar{Y}$ ) and non inverting ( $Y$ ).

The CD54AC151 and CD54ACT151 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC151 and CD74ACT151 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix).

## Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

FUNCTION TABLE

INPUTS											OUTPUTS		
$\bar{E}$	$S_2$	$S_1$	$S_0$	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$	$\bar{Y}$	$Y$
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	X
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	H	X	L	X	X	X	X	X	L	H
L	L	H	L	L	X	H	X	X	X	X	X	L	H
L	L	H	L	L	X	X	L	X	X	X	X	H	L
L	L	H	H	L	X	X	H	X	X	X	X	L	H
L	L	H	H	H	X	X	X	X	X	X	X	H	L
L	H	L	L	L	X	X	X	L	X	X	X	H	X
L	H	L	L	H	X	X	X	H	X	X	X	L	H
L	H	L	H	L	X	X	X	X	L	X	X	H	L
L	H	L	H	H	X	X	X	X	X	X	X	L	H
L	H	H	L	L	X	X	X	X	X	H	X	L	H
L	H	H	L	H	X	X	X	X	X	X	X	L	L
L	H	H	H	L	X	X	X	X	X	X	X	L	L
L	H	H	H	H	X	X	X	X	X	X	H	L	L
L	H	H	H	H	X	X	X	X	X	X	H	L	H

H = HIGH voltage level. L = LOW voltage level. X = Don't care.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	$-55$ to $+125^\circ\text{C}$
PACKAGE TYPE E, M	$-40$ to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	$-65$ to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

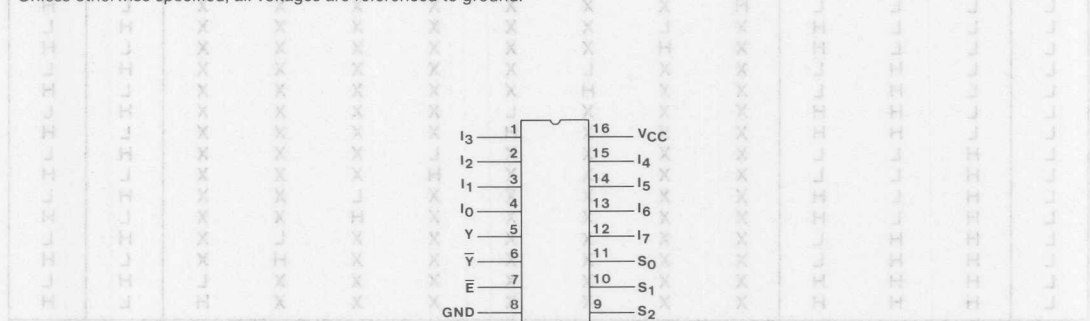
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *, (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	$-40$	$+125$	$^\circ\text{C}$
CD54 Types	$-55$	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

\*Unless otherwise specified, all voltages are referenced to ground.



HC/HCT151

92CS-38432

**TERMINAL ASSIGNMENT**

# CD54/74AC151

## CD54/74ACT151

### STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70		-40 to +125(74)		
							-40 to +85		-55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5 3.0 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V
Low-Level Input Voltage	V <sub>IL</sub>			1.5 3.0 5.5	— 0.3 0.9	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	1.5	1.40	—	1.40	—	1.40	—	V
			-0.05	3.0	2.90	—	2.90	—	2.90	—	
			-0.05	4.5	4.40	—	4.40	—	4.40	—	
			-4	3.0	2.58	—	2.48	—	2.40	—	
			-24	4.5	3.94	—	3.80	—	3.70	—	
			-75	5.5	—	—	3.85	—	—	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-50	5.5	—	—	—	—	3.85	—	V
			0.05	1.5	—	0.1	—	0.1	—	0.1	
			0.05	3.0	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3.0	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
	#		75	5.5	—	—	—	1.65	—	—	
			*	50	5.5	—	—	—	—	—	1.65
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD
1 (A)	1
2	1
3	1

Unit load is 400 pF capacitance in parallel with 1.5 kΩ resistance at 25°C.

# CD54/74AC151 CD54/74ACT151

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>	—	—	4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V <sub>IL</sub>	—	—	4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # * •	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # * •	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	—	5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	—	4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
I (All)	1
$\bar{E}$	1
S	1

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC151

## CD54/74ACT151

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ 

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C (74) -55 to +125°C (54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Any Data to Y	$t_{PLH}$ $t_{PHL}$	1.5 3.3* 5†	— 3.7 2.4	152 16.9 12.1	— 3.5 2.3	169 18.9 13.5	ns
Any Data to $\bar{Y}$	$t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 4 2.7	166 18.6 13.3	— 3.8 2.5	186 20.9 14.9	ns
Any Select to Y	$t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 5.1 3.3	204 22.5 16.3	— 4.7 3.1	228 25.5 18.2	ns
Any Select to $\bar{Y}$	$t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 5.4 3.6	219 24.5 17.5	— 5 3.4	245 27.4 19.6	ns
Any $\bar{\text{Enable}}$ to Y	$t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 3.3 2.2	137 15.3 10.9	— 3.2 2.1	153 17.1 12.2	ns
Any $\bar{\text{Enable}}$ to $\bar{Y}$	$t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 3.7 2.4	152 16.9 12.1	— 3.5 2.3	169 18.9 13.5	ns
Power Dissipation Capacitance	$C_{PD}\S$	—					pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

$\S C_{PD}$  is used to determine the dynamic power consumption, per device.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency

$C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ 

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C (74) -55 to +125°C (54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Any Data to Y	$t_{PLH}$ $t_{PHL}$	5*	2.8	13.9	2.7	15.5	ns
Any Data to $\bar{Y}$	$t_{PLH}$ $t_{PHL}$	5	3.1	15.1	2.9	16.9	ns
Any Select to Y	$t_{PLH}$ $t_{PHL}$	5	3.7	18.1	3.5	20.2	ns
Any Select to $\bar{Y}$	$t_{PLH}$ $t_{PHL}$	5	3.9	19.4	3.7	21.6	ns
Any $\bar{\text{Enable}}$ to Y	$t_{PLH}$ $t_{PHL}$	5	2.2	10.9	2.1	12.1	ns
Any $\bar{\text{Enable}}$ to $\bar{Y}$	$t_{PLH}$ $t_{PHL}$	5	2.4	12.1	2.3	13.5	ns
Power Dissipation Capacitance	$C_{PD}\S$	—					pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

min. is @ 5.5 V  
max. is @ 4.5 V

min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

$\S C_{PD}$  is used to determine the dynamic power consumption, per device.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency

$C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.



# CD54/74AC151 CD54/74ACT151

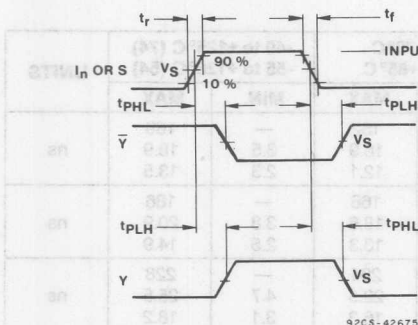


Fig. 1 - Inputs or select to output propagation delays.

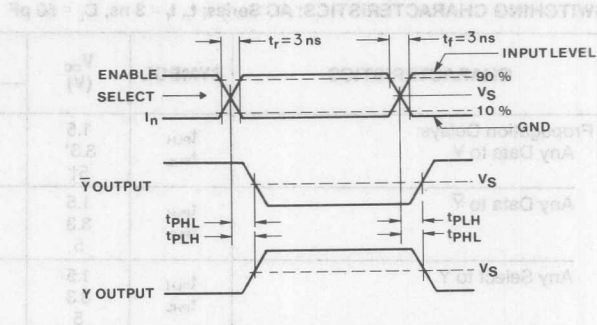


Fig. 2 - Enable to output propagation delays.

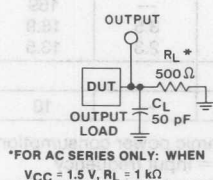


Fig. 3 - Test circuit.

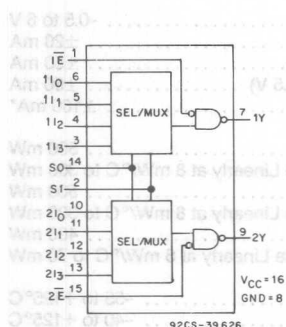
	CD54/74AC	CD54/74ACT
Input Level	V <sub>CC</sub>	3 V
Input Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	1.5 V
Output Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>

CHARACTERISTIC	SYMBOL	V <sub>CC</sub> (V)	-55 to +125°C		0 to +75°C		-55 to +125°C (typ)		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
Propagation Delay, Any Data to Y	t <sub>PLH</sub>	5	2.8	12.8	2.7	12.8	2.7	12.8	ns
Any Data to $\bar{Y}$	t <sub>PLH</sub>	5	3.1	13.1	3.0	13.1	3.0	13.1	ns
Any Select to Y	t <sub>PLH</sub>	5	3.7	13.7	3.5	13.7	3.5	13.7	ns
Any Select to $\bar{Y}$	t <sub>PLH</sub>	5	3.8	13.8	3.7	13.8	3.7	13.8	ns
Any Enable to Y	t <sub>PLH</sub>	5	5.5	15.5	5.7	15.5	5.7	15.5	ns
Any Enable to $\bar{Y}$	t <sub>PLH</sub>	5	5.4	15.4	5.3	15.4	5.3	15.4	ns
Power Dissipation Capacitance	C <sub>PD</sub>	—	—	10	—	—	—	10	pf
Input Capacitance	C <sub>I</sub>	—	—	10	—	—	—	10	pf

min is @ 5.5 V  
max is @ 4.5 V  
min is @ 5.5 V for 0 to +75°C  
max is @ 4.5 V for 0 to +75°C  
C<sub>PD</sub> is used to determine the dynamic power consumption per device  
P<sub>D</sub> = V<sub>CC</sub> · I<sub>CC</sub> (C<sub>PD</sub> + V<sub>CC</sub> · t<sub>PLH</sub>) where t<sub>PLH</sub> = input propagation delay  
C<sub>I</sub> = input load capacitance  
V<sub>CC</sub> = supply voltage

# CD54/74AC153

## CD54/74ACT153



FUNCTIONAL DIAGRAM

### Dual 4-Input Multiplexer

#### Type Features:

- Buffered inputs
- Typical propagation delay:  
6.3 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

The RCA CD54/74AC153 and CD54/74ACT153 are dual 4-input multiplexers that utilize RCA's new ADVANCED CMOS LOGIC technology. One of the four sources for each section is selected by the common Select inputs, S0 and S1. When the Enable inputs (1E, 2E) are HIGH, the outputs are in the low state.

The CD54AC153 and CD54ACT153 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC153 and CD74ACT153 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix).

#### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				ENABLE INPUTS	OUTPUT
S1	S0	nI <sub>0</sub>	nI <sub>1</sub>	nI <sub>2</sub>	nI <sub>3</sub>	nE	nY
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs S1 and S0 are common to both sections.

H = High level

L = Low level

X = Don't care

Z = High impedance

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*

**POWER DISSIPATION PER PACKAGE ( $P_D$ ):**

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at $8\text{ mW}/^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at $8\text{ mW}/^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at $6\text{ mW}/^\circ\text{C}$ to 70 mW

**OPERATING-TEMPERATURE RANGE ( $T_A$ ):**

PACKAGE TYPE F	$-55$ to $+125^\circ\text{C}$
PACKAGE TYPE E, M	$-40$ to $+125^\circ\text{C}$

**STORAGE TEMPERATURE ( $T_{stg}$ )**  $-65$  to  $+150^\circ\text{C}$ **LEAD TEMPERATURE (DURING SOLDERING):**

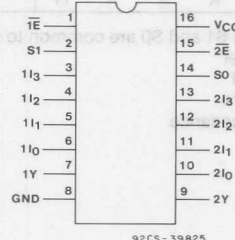
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\* (For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V
DC Input or Output Voltage, $V_i, V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40 -55	+125 +125	$^\circ\text{C}$ $^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

\* Unless otherwise specified, all voltages are referenced to ground.



92CS-39825

**TERMINAL ASSIGNMENT**

# CD54/74AC153

## CD54/74ACT153

### STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70		-40 to +125(74)		
							-40 to +85		-55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

UNIT LOADS*	INPUT
1	30 pF
0.4	30 pF

\*This load is a limit specified in static characteristics.  
Chart, e.g., 30 pF max. @ 30°C.

# CD54/74AC153 CD54/74ACT153

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS
		$V_I$ (V)	$I_O$ (mA)		+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	$V_{IH}$			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	$V_{IL}$			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
		#	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
		#	75	5.5	—	—	—	1.65	—	—	
		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	$I_I$	$V_{CC}$ or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	$I_{CC}$	$V_{CC}$ or GND		5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	$\Delta I_{CC}$	$V_{CC}-2.1$		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
S0, S1, nI <sub>0</sub> -nI <sub>3</sub> nE	1 0.47

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.



**SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$**

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: S0, S1, to Y	$t_{PLH}$	1.5	—	224	—	250	ns
	$t_{PHL}$	3.3*	5.4	25.1	5.2	28	
nl to Y	$t_{PLH}$	1.5	—	149	—	166	ns
	$t_{PHL}$	3.3	3.6	16.7	3.4	18.6	
$\overline{nE}$ to Y	$t_{PLH}$	1.5	—	133	—	148	ns
	$t_{PHL}$	3.3	3.2	14.8	3.1	16.5	
Power Dissipation Capacitance	$C_{PD}\S$	—	—	—	—	—	pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

$\S C_{PD}$  is used to determine the dynamic power consumption, per multiplexer.  
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

**SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$**

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: S0, S1, to Y	$t_{PLH}$	5†	3.9	19.3	3.8	22	ns
	$t_{PHL}$	5	3.3	16.2	3.1	18	
nl to Y	$t_{PLH}$	5	3.3	16.2	3.1	18	ns
	$t_{PHL}$	5	3.3	16.2	3.1	18	
$\overline{nE}$ to Y	$t_{PLH}$	5	2.3	11.3	2.1	12.6	ns
	$t_{PHL}$	5	2.3	11.3	2.1	12.6	
Power Dissipation Capacitance	$C_{PD}\S$	—	—	—	—	—	pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

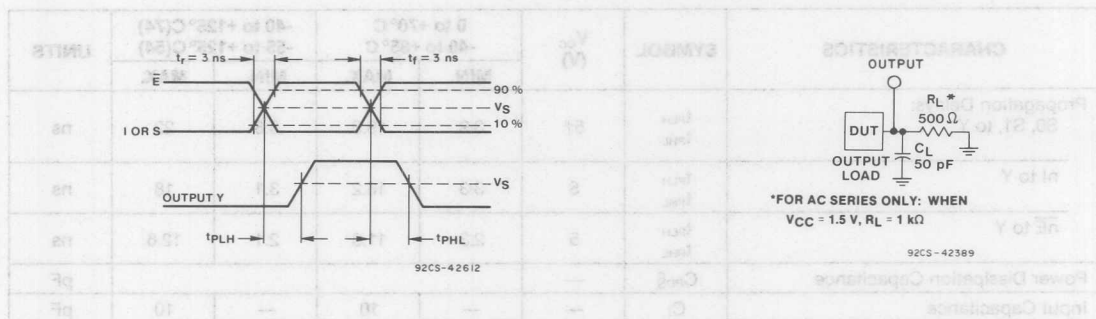
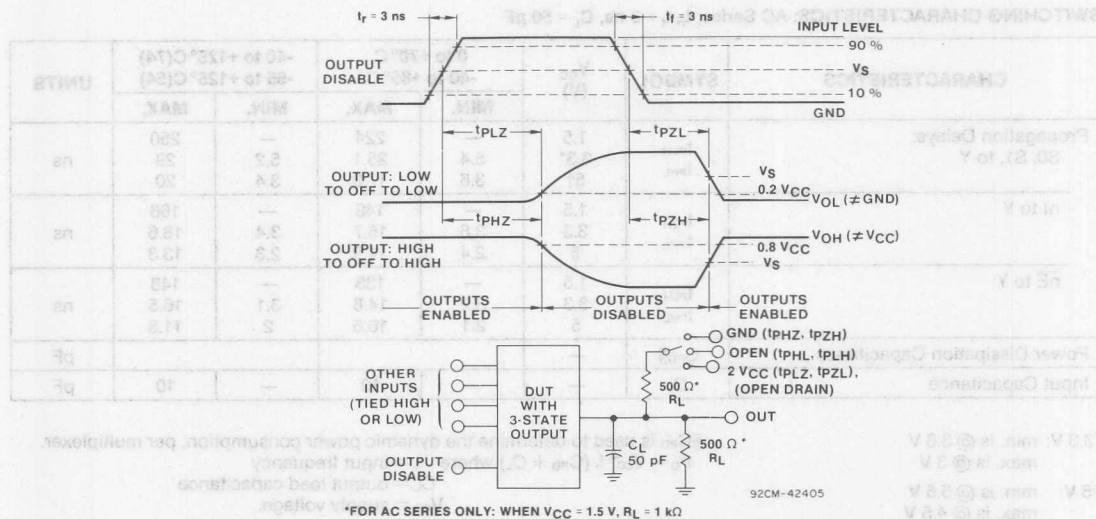
†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

$\S C_{PD}$  is used to determine the dynamic power consumption, per multiplexer.  
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

Output Switching Voltage $V_{OS}$	Input Switching Voltage $V_{IS}$	Input Level
0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>	0 V
0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>	1 V
0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>	1.5 V
0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>	2 V

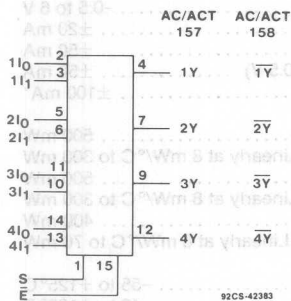
# CD54/74AC153 CD54/74ACT153



	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_s$	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, $V_s$	$0.5 V_{CC}$	$0.5 V_{CC}$

Advance Information

# CD54/74AC157, CD54/74AC158 CD54/74ACT157, CD54/74ACT158



## Quad 2-Input Multiplexers

AC/ACT157 - Non-Inverting  
AC/ACT158 - Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay (AC/ACT158):  
3.8 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

### FUNCTIONAL DIAGRAM

The GE/RCA CD54/74AC157, -158 and CD54/74ACT157, -158 are quad 2-input multiplexers utilizing GE/RCA's new ADVANCED CMOS LOGIC technology. Both circuits can select four bits of data from two sources under the control of a common select input (S). The Enable input ( $\bar{E}$ ) is active LOW. When  $\bar{E}$  is HIGH, all of the outputs of the 158 are forced HIGH and in the 157, all of the outputs are forced LOW, regardless of all other input conditions.

The CD54AC/ACT157 and CD54AC/ACT158 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT157 and CD74AC/ACT158 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

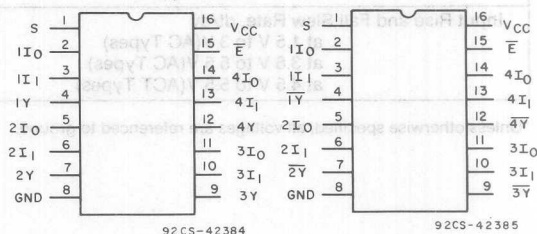
\*FAST is a Trademark of Fairchild Semiconductor Corp.

### TERMINAL ASSIGNMENT DIAGRAMS

### TRUTH TABLE

Enable	Select Input	Data Inputs		Output	
		$I_0$	$I_1$	157	158
$\bar{E}$	S			Y	$\bar{Y}$
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High level, L = Low level, X = Don't care



CD54/74AC/ACT157

CD54/74AC/ACT158

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	..... -0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	..... $\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	..... $\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	..... $\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	..... $\pm 100$ mA*

**POWER DISSIPATION PER PACKAGE ( $P_D$ ):**

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	..... 500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	..... Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	..... 500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	..... Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	..... 400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	..... Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW

**OPERATING-TEMPERATURE RANGE ( $T_A$ ):**

PACKAGE TYPE F	..... -55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	..... -40 to $+125^\circ\text{C}$

STORAGE TEMPERATURE ( $T_{stg}$ )	..... -65 to $+150^\circ\text{C}$
-----------------------------------	-----------------------------------

**LEAD TEMPERATURE (DURING SOLDERING):**

At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	..... $+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	..... $+300^\circ\text{C}$

\* (For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A =$ Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40 -55	+125 +125	$^\circ\text{C}$ $^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

\* Unless otherwise specified, all voltages are referenced to ground.

# CD54/74AC157, CD54/74AC158

## CD54/74ACT157, CD54/74ACT158

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70		-40 to +125(74)		
							-40 to +85		-55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>		—	1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V <sub>IL</sub>		—	1.5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
			Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	
0.05	3	—	0.1	—	0.1	—	0.1	—	0.1		
0.05	4.5	—	0.1	—	0.1	—	0.1	—	0.1		
12	3	—	0.36	—	0.44	—	0.5	—	0.5		
24	4.5	—	0.36	—	0.44	—	0.5	—	0.5		
75	5.5	—	—	—	1.65	—	—	—	1.65		
50	5.5	—	—	—	—	—	—	—	1.65		
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

INPUT	OUTPUT	UNIT
157	158	(A)
0.07	0.07	5
0.00	0.00	2
1.38	1.38	

\*Unit load is  $\Delta I_{CC}$  limit specified in Static  
Characteristic Chart, eq. 5, 4 mA max. @ 25°C.



# CD54/74AC157, CD54/74AC158 CD54/74ACT157, CD54/74ACT158

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS
			+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	$V_{IH}$	4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	$V_{IL}$	4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	4.4	—	4.4	—	4.4	—	V
		#	3.94	—	3.8	—	3.7	—	
		*	—	—	3.85	—	—	—	
		*	—	—	—	—	3.85	—	
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.1	—	0.1	—	0.1	—	V
		#	0.36	—	0.44	—	0.5	—	
		*	—	—	1.65	—	—	—	
		*	—	—	—	—	1.65	—	
Input Leakage Current	$I_I$	$V_{CC}$ or GND	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	$I_{CC}$	$V_{CC}$ or GND	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	$\Delta I_{CC}$	$V_{CC}-2.1$	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*	
	157	158
I (All)	0.37	0.37
$\bar{E}$	0.83	0.83
S	1.33	1.33

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC157, CD54/74AC158

## CD54/74ACT157, CD54/74ACT158

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ 

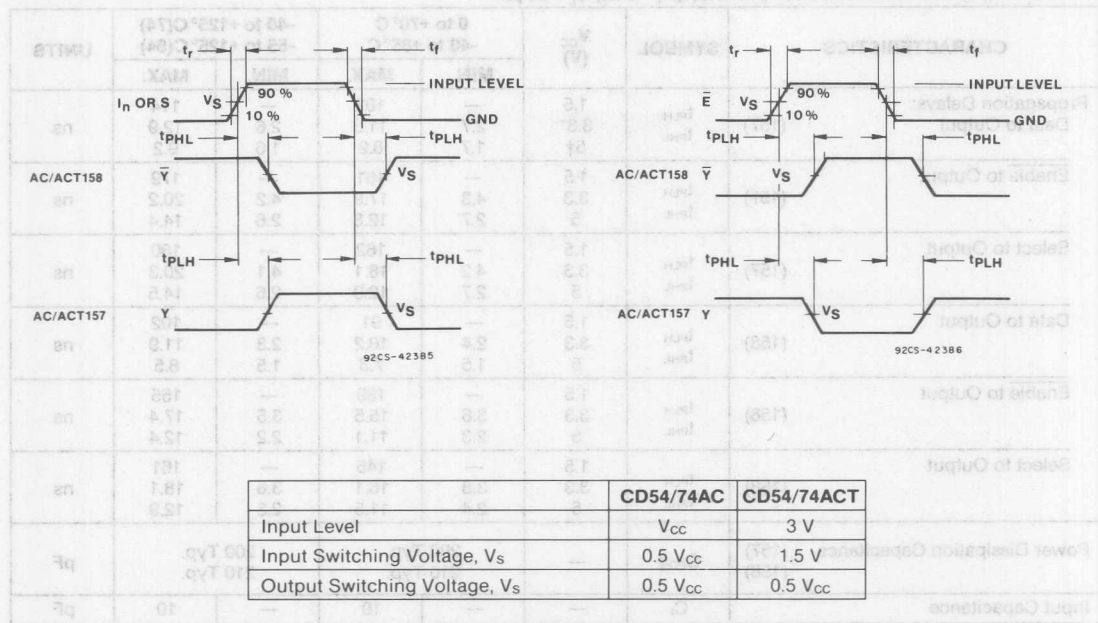
CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output	(157) $t_{PLH}$ $t_{PHL}$	1.5 3.3* 5†	— 2.7 1.7	102 11.5 8.2	— 2.6 1.6	114 12.9 9.2	ns
Enable to Output	(157) $t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 4.3 2.7	161 17.9 12.8	— 4.2 2.6	179 20.2 14.4	ns
Select to Output	(157) $t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 4.2 2.7	162 18.1 12.9	— 4.1 2.6	180 20.3 14.5	ns
Data to Output	(158) $t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 2.4 1.5	91 10.2 7.3	— 2.3 1.5	102 11.9 8.5	ns
Enable to Output	(158) $t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 3.6 2.3	139 15.5 11.1	— 3.5 2.2	155 17.4 12.4	ns
Select to Output	(158) $t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 3.8 2.4	145 16.1 11.5	— 3.6 2.3	161 18.1 12.9	ns
Power Dissipation Capacitance	(157) (158) $C_{PD}\S$	—	200 Typ. 210 Typ.		200 Typ. 210 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ 

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output	(157) $t_{PLH}$ $t_{PHL}$	5†	2.1	10.1	2	11.2	ns
Enable to Output	(157) $t_{PLH}$ $t_{PHL}$	5	2.7	13.2	2.6	14.8	ns
Select to Output	(157) $t_{PLH}$ $t_{PHL}$	5	2.8	13.3	2.7	14.9	ns
Data to Output	(158) $t_{PLH}$ $t_{PHL}$	5	1.8	8.4	1.7	9.4	ns
Enable to Output	(158) $t_{PLH}$ $t_{PHL}$	5	2.4	11.1	2.3	12.4	ns
Select to Output	(158) $t_{PLH}$ $t_{PHL}$	5	2.4	11.5	2.3	12.9	ns
Power Dissipation Capacitance	(157) (158) $C_{PD}\S$	—	295 Typ. 345 Typ.		295 Typ. 345 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V†5 V: min. is @ 5.5 V  
max. is @ 4.5 V5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C§ $C_{PD}$  is used to determine the dynamic power consumption, per function.For AC Series,  $PD = C_{PD}V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o)$ For ACT Series,  $PD = C_{PD}V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o) + V_{CC}\Delta I_{CC}$ where  $f_i$  = input frequency $f_o$  = output frequency $C_L$  = output load capacitance $V_{CC}$  = supply voltage.

CD54/74AC157, CD54/74AC158  
CD54/74ACT157, CD54/74ACT158



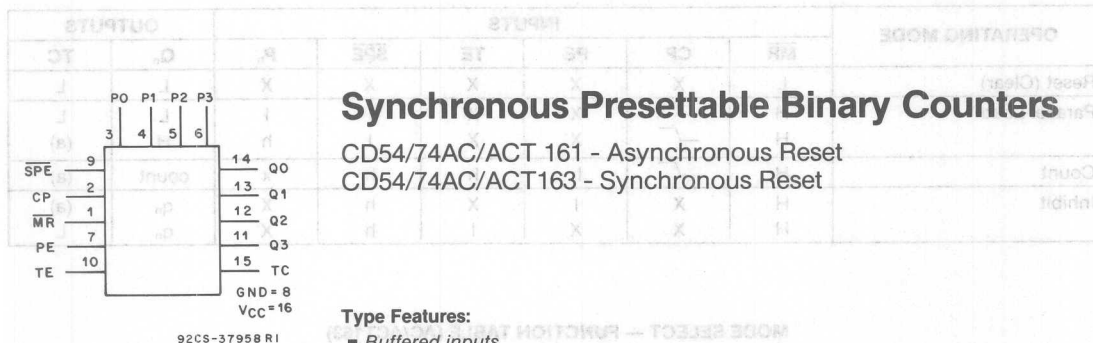
CHARACTERISTICS	SYMBOL	UNIT	-40 to +85°C		-55 to +125°C (typ)	
			MIN.	MAX.	MIN.	MAX.
Propagation Delay: Data to Output (157)	$t_{PD}$	ns	5.1	10.1	5	11.2
Enable to Output (157)	$t_{EPO}$	ns	5.7	13.2	5.6	14.8
Select to Output (157)	$t_{SPO}$	ns	5.8	13.3	5.7	14.9
Data to Output (158)	$t_{PD}$	ns	1.8	8.4	1.7	9.4
Enable to Output (158)	$t_{EPO}$	ns	2.4	11.1	2.3	12.4
Select to Output (158)	$t_{SPO}$	ns	2.4	11.2	2.3	12.9
Power Dissipation Capacitance (157)	$C_{PD}$	pf	—	500 Typ	—	500 Typ
Input Capacitance (157)	$C_I$	pf	—	10	—	10

$V_{CC}$  = supply voltage  
 $C_L$  = output load capacitance  
 $f$  = output frequency  
 $f_i$  = input frequency  
where  $t_i$  = input delay  
For ACT Series,  $P_D = C_{PD} V_{CC}^2 (f_i + 2f_o) + V_{CC} \Delta f_o$   
For AC Series,  $P_D = C_{PD} V_{CC}^2 (f_i + 2f_o)$   
For AC Series,  $P_D = C_{PD} V_{CC}^2 (f_i + 2f_o)$   
 $G_{PM}$  is used to determine the dynamic power consumption, per function

15 V: min is @ 3.5 V  
max is @ 4.5 V  
12 V: min is @ 3.5 V  
max is @ 4.5 V  
5 V: min is @ 3.5 V for 0 to +70°C  
max is @ 4.5 V for 0 to +70°C

Product Preview

# CD54/74AC161, CD54/74AC163 CD54/74ACT161, CD54/74ACT163



**FUNCTIONAL DIAGRAM**

The RCA CD54/74AC161, -163 and CD54/74ACT161, -163 are synchronous presettable binary counters that utilize RCA's new ADVANCED CMOS LOGIC technology. The CD54/74AC/ACT161 are asynchronously reset; the CD54/74AC/ACT163 devices are reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

A LOW level on the Synchronous Parallel Enable input, SPE, disables the counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for SPE are met).

The counters are reset with a LOW level on the Master Reset input, MR. In the CD54/74AC/ACT163 counter (synchronous reset), the requirements for setup and hold time with respect to the clock must be met.

Two count enables, PE and TE, in each counter are provided for n-bit cascading. Reset action occurs regardless of the level of the SPE, PE, and TE inputs (and the clock input, CP, in the CD54/74AC/ACT161).

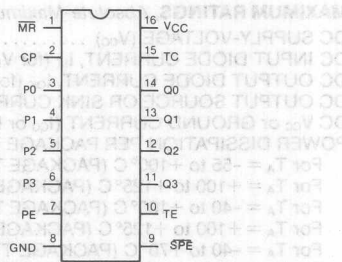
The look-ahead carry feature simplifies serial cascading of the counters. Both count enable inputs (PE and TE) must be HIGH to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count, the terminal count (TC) output goes HIGH for one clock period. This TC pulse is used to enable the next cascaded stage.

The CD54AC/ACT161 and CD54AC/ACT163 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT161 and CD74AC/ACT163 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix).

**Family Features:**




- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/IS with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24$ -mA output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.







**TERMINAL ASSIGNMENT**

MODE SELECT — FUNCTION TABLE (AC/ACT161)

OPERATING MODE	INPUTS						OUTPUTS	
	MR	CP	PE	TE	SPE	P <sub>n</sub>	Q <sub>n</sub>	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H		X	X	l	l	L	L
	H		X	X	l	h	H	(a)
Count	H		h	h	h	x	count	(a)
Inhibit	H	X	l	X	h	X	q <sub>n</sub>	(a)
	H	X	X	l	h	X	q <sub>n</sub>	L

MODE SELECT — FUNCTION TABLE (AC/ACT163)

OPERATING MODE	INPUTS						OUTPUTS	
	MR	CP	PE	TE	SPE	P <sub>n</sub>	Q <sub>n</sub>	TC
Reset (Clear)	l		X	X	X	X	L	L
Parallel Load	h		X	X	l	l	L	L
	h		X	X	l	h	H	(a)
Count	h		h	h	h	X	count	(a)
Inhibit	h	X	l	X	h	X	q <sub>n</sub>	(a)
	h	X	X	l	h	X	q <sub>n</sub>	L

H = HIGH voltage level steady state.


L = LOW voltage level steady state.

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.

X = Don't care.

q = Lowercase letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.

 = LOW-to-HIGH clock transition.

## NOTE:

(a) The TC output is HIGH when TE is HIGH and the counter is at Terminal Count (HHHH).

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V<sub>CC</sub>) ..... -0.5 to 6 VDC INPUT DIODE CURRENT, I<sub>IK</sub> (for V<sub>I</sub> < -0.5 V or V<sub>I</sub> > V<sub>CC</sub> + 0.5 V) ..... ±20 mADC OUTPUT DIODE CURRENT, I<sub>OK</sub> (for V<sub>O</sub> < -0.5 V or V<sub>O</sub> > V<sub>CC</sub> + 0.5 V) ..... ±50 mADC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I<sub>O</sub> (for V<sub>O</sub> > -0.5 V or V<sub>O</sub> < V<sub>CC</sub> + 0.5 V) ..... ±50 mADC V<sub>CC</sub> or GROUND CURRENT (I<sub>CC</sub> or I<sub>GND</sub>) ..... ±100 mA\*POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):For T<sub>A</sub> = -55 to +100°C (PACKAGE TYPE F) ..... 500 mWFor T<sub>A</sub> = +100 to +125°C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/°C to 300 mWFor T<sub>A</sub> = -40 to +100°C (PACKAGE TYPE E) ..... 500 mWFor T<sub>A</sub> = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mWFor T<sub>A</sub> = -40 to +70°C (PACKAGE TYPE M) ..... 400 mWFor T<sub>A</sub> = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mWOPERATING-TEMPERATURE RANGE (T<sub>A</sub>):

PACKAGE TYPE F ..... -55 to +125°C

PACKAGE TYPE E, M ..... -40 to +125°C

STORAGE TEMPERATURE (T<sub>stg</sub>) ..... -65 to +150°C

## LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C

Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

\*(For up to 4 outputs per device; add ± 25 mA for each additional output.)



# CD54/74AC161, CD54/74AC163

## CD54/74ACT161, CD54/74ACT163

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5	5.5	V
	4.5	5.5	V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40	+125	°C
	-55	+125	°C
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0	50	ns/V
	0	20	ns/V
	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

**STATIC ELECTRICAL CHARACTERISTICS: AC Series**

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
				+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)			
	V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V <sub>IH</sub>		1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V	
Low-Level Input Voltage	V <sub>IL</sub>		1.5 3 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05 -0.05 -0.05 -4 -24 -75 -50	1.5 3 4.5 3 4.5 5.5 5.5	1.4 2.9 4.4 2.58 3.94 — —	— — — — — — —	1.4 2.9 4.4 2.48 3.8 3.85 —	— — — — — — —	1.4 2.9 4.4 2.4 3.7 — 3.85	— — — — — — —	V
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05 0.05 0.05 12 24 75 50	1.5 3 4.5 3 4.5 5.5 5.5	— — — — — — —	0.1 0.1 0.1 0.36 0.36 — —	— — — — — — —	0.1 0.1 0.1 0.44 0.44 1.65 —	— — — — — — —	0.1 0.1 0.1 0.5 0.5 — 1.65	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# CD54/74AC161, CD54/74AC163 CD54/74ACT161, CD54/74ACT163

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> Or V <sub>IL</sub> # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load		ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

### ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
Pn	0.13
CP	1
MR, TE	0.83
SPE	0.67
PE	0.5

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC161, CD54/74AC163

## CD54/74ACT161, CD54/74ACT163

## PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Max. CP Frequency	f <sub>max</sub>	1.5 3.3* 5†	6.5 46 82	—	6 42 75	—	MHz
CP Pulse Width	t <sub>w</sub>	1.5 3.3 5	77 10.9 6.1	—	84 11.9 6.7	—	ns
SPE HIGH (Count)							
SPE LOW (Load)	t <sub>w</sub>	1.5 3.3 5	—	—	—	—	ns
MR Pulse Width (161)	t <sub>w</sub>	1.5 3.3 5	—	—	—	—	ns
Setup Time Pn to CP	t <sub>su</sub>	1.5 3.3 5	—	—	—	—	ns
PE or TE to CP	t <sub>su</sub>	1.5 3.3 5	—	—	—	—	ns
SPE or MR to CP (163)	t <sub>su</sub>	1.5 3.3 5	—	—	—	—	ns
Hold Time Pn to CP	t <sub>H</sub>	1.5 3.3 5	—	—	—	—	ns
PE or TE to CP	t <sub>H</sub>	1.5 3.3 5	—	—	—	—	ns
SPE or MR to CP (163)	t <sub>H</sub>	1.5 3.3 5	—	—	—	—	ns
Recovery Time MR to CP (161)	t <sub>REC</sub>	1.5 3.3 5	—	—	—	—	ns

\*3.3 V: min. is @ 3 V

†5 V: min is @ 4.5 V

5 V: min. is @ 4.75 V for 0 to +70°C

# CD54/74AC161, CD54/74AC163 CD54/74ACT161, CD54/74ACT163

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn (SPE HIGH)	$t_{PLH}$	1.5	—	185	—	207	ns
	$t_{PHL}$	3.3*	4.5	20.7	4.3	23.1	
		5†	3	14.8	2.8	16.5	
CP to Qn (SPE LOW)	$t_{PLH}$	1.5	—	185	—	207	ns
	$t_{PHL}$	3.3	4.5	20.7	4.3	23.1	
		5	3	14.8	2.8	16.5	
CP to TC	$t_{PLH}$	1.5	—	188	—	209	ns
	$t_{PHL}$	3.3	4.5	21	4.4	23.4	
		5	3	15	2.9	16.7	
TE to TC	$t_{PLH}$	1.5	—	119	—	129	ns
	$t_{PHL}$	3.3	2.9	13.3	2.6	14.4	
		5	1.9	9.5	1.8	10.3	
$\overline{MR}$ to Qn (161)	$t_{PLH}$	1.5	—	185	—	207	ns
	$t_{PHL}$	3.3	4.5	20.7	4.3	23.1	
		5	3	14.8	2.8	16.5	
$\overline{MR}$ to TC (161)	$t_{PLH}$	1.5	—	185	—	207	ns
	$t_{PHL}$	3.3	4.5	20.7	4.3	23.1	
		5	3	14.8	2.8	16.5	
Power Dissipation Capacitance	$C_{PD}\S$	—	—	—	—	—	pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V.  
max. is @ 3 V.

†5 V: min. is @ 5.5 V.  
max. is @ 4.5 V.

min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

$\S C_{PD}$  is used to determine the dynamic power consumption, per flip-flop.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$  where  $f_i$  = input frequency  
 $f_o$  = output frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

# CD54/74AC161, CD54/74AC163

## CD54/74ACT161, CD54/74ACT163

## PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Max. CP Frequency	f <sub>max</sub>	5*	82	—	75	—	MHz
CP Pulse Width	t <sub>w</sub>	5	6.1	—	6.7	—	ns
SPE HIGH (Count)	t <sub>w</sub>	5	—	—	—	—	ns
SPE LOW (Load)	t <sub>w</sub>	5	—	—	—	—	ns
MR Pulse Width	t <sub>w</sub>	5	—	—	—	—	ns
Setup Time	t <sub>su</sub>	5	—	—	—	—	ns
Pn to CP		5	—	—	—	—	
PE or TE to CP		5	—	—	—	—	
SPE or MR to CP (163)		5	—	—	—	—	
Hold Time	t <sub>h</sub>	5	—	—	—	—	ns
Pn to CP		5	—	—	—	—	
PE or TE to CP		5	—	—	—	—	
SPE or MR to CP (163)		5	—	—	—	—	
Recovery Time	t <sub>rec</sub>	5	—	—	—	—	ns
MR TO CP (161)							

\*5 V: Min. is @ 4.5 V

5 V: Min. is @ 4.75 V for 0 to +70°C

SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:	t <sub>PLH</sub> t <sub>PHL</sub>	5*	3	14.8	2.8	16.5	ns
CP to Qn							
(SPE HIGH)							
CP to Qn		5	3	14.8	2.8	16.5	
(SPE LOW)							
CP to TC		5	3	15	2.9	16.7	
TE to TC		5	2	10	1.8	10.8	ns
MR to Qn (161)		5	3	14.8	2.8	16.5	ns
MR to TC (161)		5	3	14.8	2.8	16.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> †	—	—	—	—	—	pF
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF

\*5 V: min. is @ 5.5 V

max. is @ 4.5 V.

5 V: min. is @ 5.25 V for 0 to +70°C

max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per flip-flop.P<sub>D</sub> = C<sub>PD</sub>V<sub>CC</sub><sup>2</sup>f<sub>i</sub> + Σ(C<sub>L</sub>V<sub>CC</sub><sup>2</sup>f<sub>o</sub>) + V<sub>CC</sub>ΔI<sub>CC</sub> where f<sub>i</sub> = input frequencyf<sub>o</sub> = output frequencyC<sub>L</sub> = output load capacitanceV<sub>CC</sub> = supply voltage.



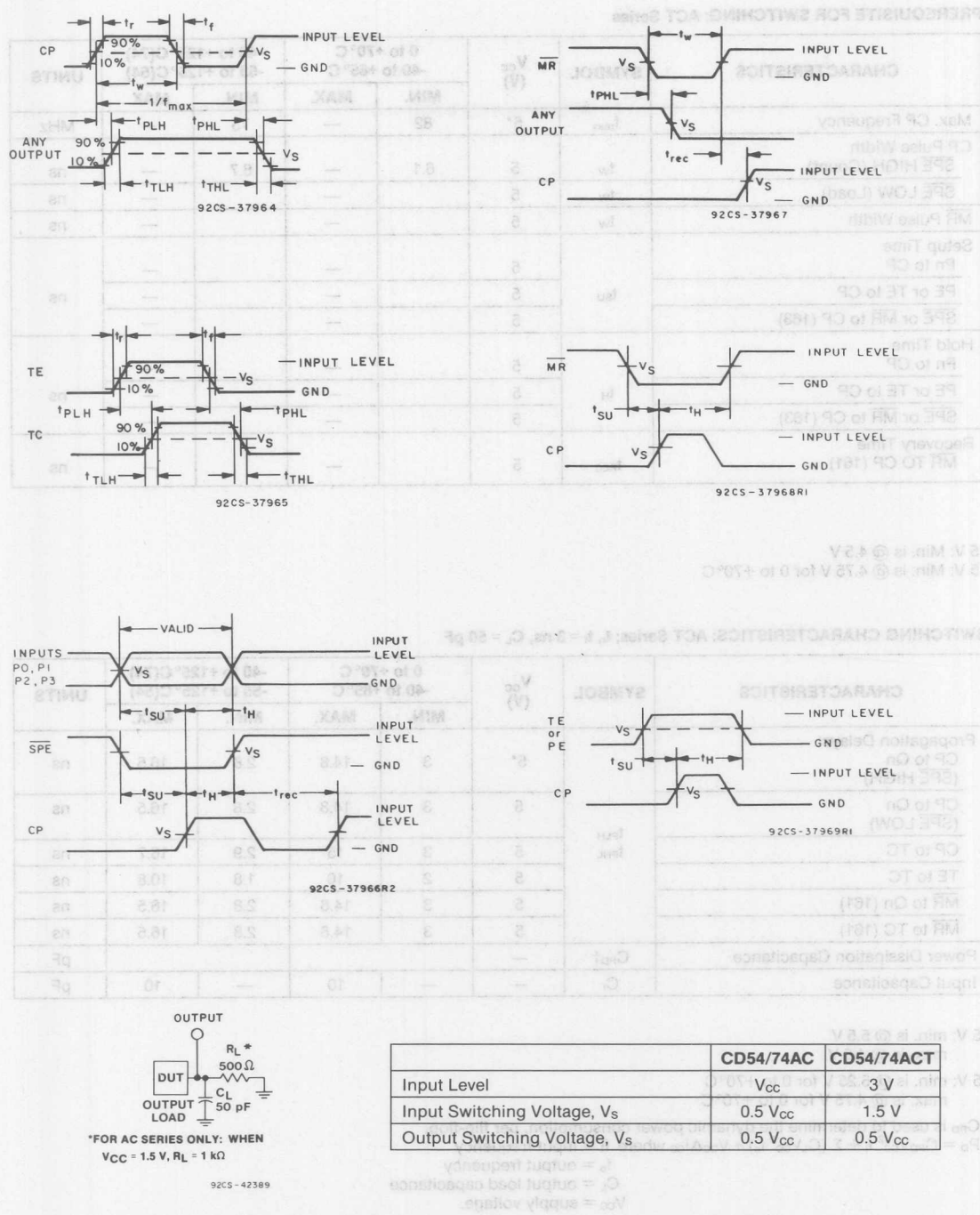


Fig. 1 - Propagation delay times, setup, hold, and recovery times, and test circuit.

# CD54/74AC161, CD54/74AC163 CD54/74ACT161, CD54/74ACT163

Sequence illustrated in waveforms

1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

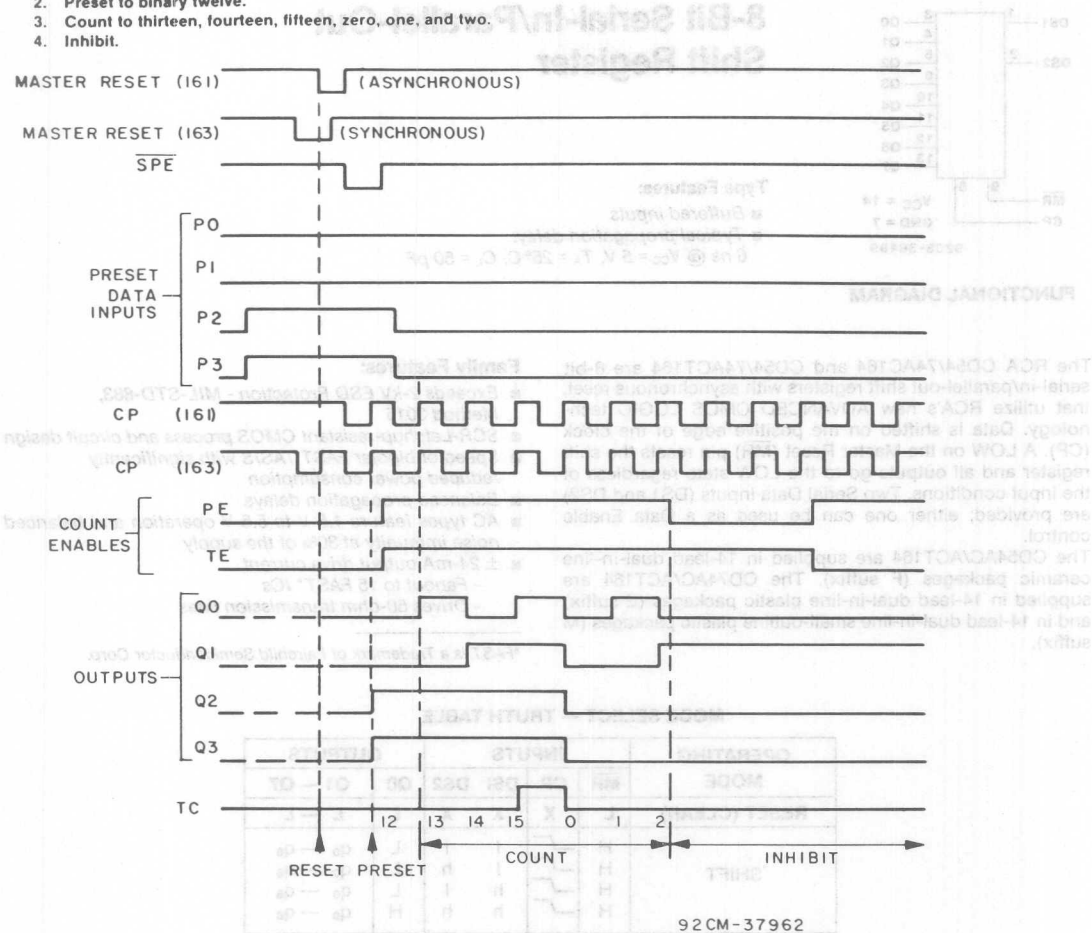
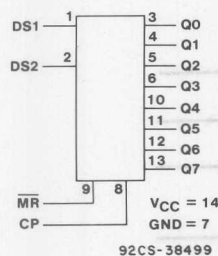


Fig. 2 - Timing diagrams for the CD54/74AC/ACT 161 and 163.

# CD54/74AC164

## CD54/74ACT164

Product Preview



## 8-Bit Serial-In/Parallel-Out Shift Register

### Type Features:

- Buffered inputs
- Typical propagation delay:  
6 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

### FUNCTIONAL DIAGRAM

The RCA CD54/74AC164 and CD54/74ACT164 are 8-bit serial-in/parallel-out shift registers with asynchronous reset, that utilize RCA's new ADVANCED CMOS LOGIC technology. Data is shifted on the positive edge of the clock (CP). A LOW on the Master Reset (MR) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (DS1 and DS2) are provided; either one can be used as a Data Enable control.

The CD54AC/ACT164 are supplied in 14-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT164 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	MR	CP	DS1	DS2	Q0	Q1 — Q7
RESET (CLEAR)	L	X	X	X	L	L — L
SHIFT	H	—	l	l	L	$q_0$ — $q_6$
	H	—	l	h	L	$q_0$ — $q_6$
	H	—	h	l	L	$q_0$ — $q_6$
	H	—	h	h	H	$q_0$ — $q_6$

H = HIGH voltage level.

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.

L = LOW voltage level.

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.

q = Lower case letters indicate the state of the reference input (or output) one setup time prior to the LOW-to-HIGH clock transition.

X = Don't care.

— = LOW-to-HIGH clock transition.

Technical Data

# CD54/74AC164

## CD54/74ACT164

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6.0 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*

### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW

### OPERATING-TEMPERATURE RANGE ( $T_A$ ):

PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$

### STORAGE TEMPERATURE ( $T_{stg}$ ):

	-65 to $+150^\circ\text{C}$
--	-----------------------------

### LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

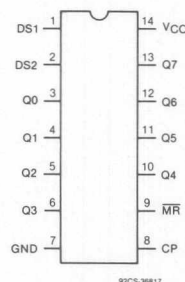
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

### RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)		20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.



TERMINAL ASSIGNMENT

# STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70		-40 to +125(74)		
							-40 to +85		-55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.



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# CD54/74AC164 CD54/74ACT164

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> #	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			*	-50	5.5	—	—	—	—	3.85	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> #	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			*	50	5.5	—	—	—	—	—	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

### ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
DS1, DS2	0.5
MR	0.74
CP	0.71

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC164 CD54/74ACT164

## PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f <sub>MAX</sub>	1.5 3.3* 5†	—	—	—	—	MHz
MR Pulse Width	t <sub>w</sub>	1.5 3.3 5	—	—	—	—	ns
CP Pulse Width	t <sub>w</sub>	1.5 3.3 5	—	—	—	—	ns
Setup Time	t <sub>SU</sub>	1.5 3.3 5	—	—	—	—	ns
Hold Time	t <sub>H</sub>	1.5 3.3 5	—	—	—	—	ns
MR to CP Removal Time	t <sub>REM</sub>	1.5 3.3 5	—	—	—	—	ns

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

5 V: min is @ 4.75 V for 0 to +70°C

## SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn	t <sub>PLH</sub>	1.5	—	140	—	157	ns
	t <sub>PHL</sub>	3.3*	3.5	15.7	3.2	17.5	
	t <sub>PHL</sub>	5†	2.3	11.2	2.1	12.5	
MR to Qn	t <sub>PLH</sub>	1.5	—	157	—	174	ns
	t <sub>PHL</sub>	3.3	3.9	17.5	3.7	19.5	
	t <sub>PHL</sub>	5	2.6	12.5	2.4	13.9	
Power Dissipation Capacitance	C <sub>PD</sub> §	—	—	—	—	—	pF
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per device.

P<sub>D</sub> = C<sub>PD</sub>V<sub>CC</sub><sup>2</sup> f<sub>i</sub> + Σ (C<sub>L</sub> V<sub>CC</sub><sup>2</sup> f<sub>o</sub>) where  
f<sub>i</sub> = input frequency  
f<sub>o</sub> = output frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.

# CD54/74AC164

## CD54/74ACT164

### PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f <sub>max</sub>	5*		—		—	MHz
MR Pulse Width	t <sub>w</sub>	5		—		—	ns
CP Pulse Width	t <sub>w</sub>	5		—		—	ns
Setup Time	t <sub>SU</sub>	5		—		—	ns
Hold Time	t <sub>H</sub>	5		—		—	ns
Removal Time	t <sub>REM</sub>	5		—		—	ns

\*Min. is @ 4.5 V

Min. is @ 4.75 V for 0 to +70°C

### SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn	t <sub>PLH</sub>	5*	2.7	13.3	2.6	14.9	ns
MR Qn	t <sub>PHL</sub>	5	2.9	14.2	2.7	15.8	
Power Dissipation Capacitance	C <sub>PD</sub> †	—					pF
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF

\*5 V: min. is @ 5.5 V  
max. is @ 4.5 V.

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

†C<sub>PD</sub> is used to determine the dynamic power consumption, per device.

P<sub>D</sub> = C<sub>PD</sub>V<sub>CC</sub><sup>2</sup> f<sub>i</sub> + Σ (C<sub>L</sub>V<sub>CC</sub><sup>2</sup> f<sub>o</sub>) + V<sub>CC</sub> ΔI<sub>CC</sub>, where f<sub>i</sub> = input frequency  
f<sub>o</sub> = output frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.

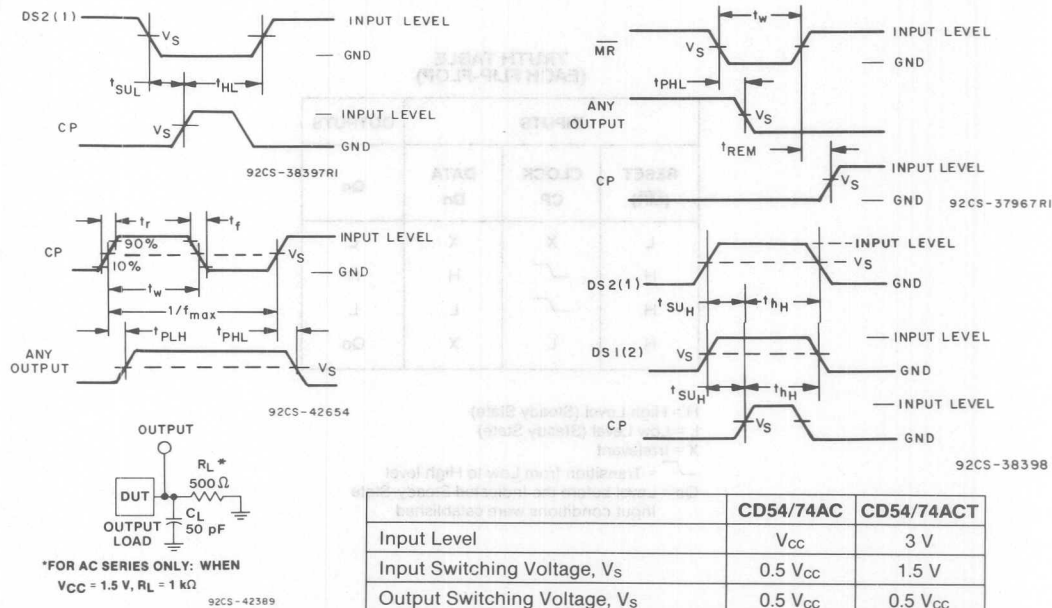
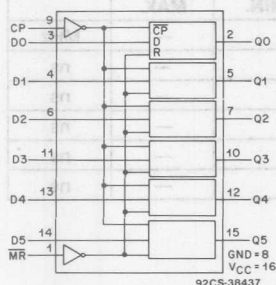


Fig. 1 - Propagation delay times, setup and hold times, removal times, and test circuit.



FUNCTIONAL DIAGRAM

The RCA CD54/74ACT174 and CD54/74ACT174 are hex D flip-flops with reset that utilize RCA's new ADVANCED CMOS LOGIC technology. Information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. All six flip-flops are controlled by a common clock (CP) and a common reset (MR). Resetting is accomplished by a low-voltage level independent of the clock.

The CD54AC174 and CD54ACT174 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC174 and CD74ACT174 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix).

## Hex D Flip-Flop with Reset

### Type Features:

- Buffered inputs
- Typical propagation delay:  
6.4 ns @  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50 pF$

### Family Features:

- Exceeds 2-kV ESD Protection — MIL-STD 883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST\*AS/S with significantly reduced power consumption
- Balanced Propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- $\pm 24 mA$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE  
(EACH FLIP-FLOP)

INPUTS			OUTPUTS
RESET (MR)	CLOCK CP	DATA Dn	Qn
L	X	X	L
H	X	H	H
H	X	L	L
H	L	X	Qo

H = High Level (Steady State)

L = Low Level (Steady State)

X = Irrelevant

— = Transition from Low to High level

Qo = Level before the Indicated Steady-State  
Input conditions were established

# CD54/74AC174 CD54/74ACT174

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

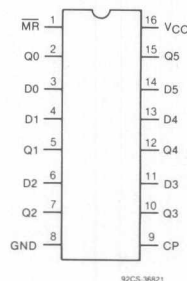
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *:			
(For $T_A =$ Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I, V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.



TOP VIEW  
TERMINAL ASSIGNMENT



# CD54/74AC174 CD54/74ACT174

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
				+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.



# CD54/74AC174 CD54/74ACT174

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C								UNITS
			+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	$V_{IH}$		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	$V_{IL}$		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$ # *	4.5	4.4	—	4.4	—	4.4	—	V	
			4.5	3.94	—	3.8	—	3.7	—		
			5.5	—	—	3.85	—	—	—		
			5.5	—	—	—	—	3.85	—		
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$ # *	4.5	—	0.1	—	0.1	—	0.1	V	
			4.5	—	0.36	—	0.44	—	0.5		
			5.5	—	—	—	1.65	—	—		
			5.5	—	—	—	—	—	1.65		
Input Leakage Current	$I_I$	$V_{CC}$ or GND	5.5	—	±0.1	—	±1	—	±1	μA	
Quiescent Supply Current, MSI	$I_{CC}$	$V_{CC}$ or GND	5.5	—	8	—	80	—	160	μA	
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	$\Delta I_{CC}$	$V_{CC}-2.1$	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

### ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
Dn, MR	0.5
CP	0.83

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t <sub>su</sub>	1.5 3.3* 5†	—	—	—	—	ns
Hold Time	t <sub>h</sub>	1.5 3.3 5	—	—	—	—	ns
Removal Time MR to CP	t <sub>rem</sub>	1.5 3.3 5	—	—	—	—	ns
MR Pulse Width	t <sub>w</sub>	1.5 3.3 5	—	—	—	—	ns
CP Pulse Width	t <sub>w</sub>	1.5 3.3 5	—	—	—	—	ns
CP Frequency	f <sub>max</sub>	1.5 3.3 5	—	—	—	—	MHz

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

5 V: min is @ 4.75 V for 0 to +70°C

## SWITCHING CHARACTERISTICS: AC Series; t<sub>p</sub>, t<sub>r</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn	t <sub>PLH</sub>	1.5 3.3*	—	152	—	169	ns
	t <sub>PHL</sub>	5†	3.6 2.4	16.9 12.1	3.5 2.3	18.9 13.5	
MR to Qn	t <sub>PLH</sub>	1.5 3.3	—	144	—	159	ns
	t <sub>PHL</sub>	5	3.5 2.3	16.1 11.5	3.4 2.2	17.8 12.7	
Power Dissipation Capacitance	C <sub>PD</sub> §	—	—	—	—	—	pF
Input Capacitance	C <sub>i</sub>	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per flip-flop.

P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>i</sub> + Σ (C<sub>L</sub> V<sub>CC</sub><sup>2</sup> f<sub>o</sub>) where f<sub>i</sub> = input frequency

f<sub>o</sub> = output frequency

C<sub>L</sub> = output load capacitance

V<sub>CC</sub> = supply voltage.

# CD54/74AC174

## CD54/74ACT174

### PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t <sub>SU</sub>	5†		—		—	ns
Hold Time	t <sub>H</sub>	5		—		—	ns
Removal Time MR to CP	t <sub>REM</sub>	5		—		—	ns
MR Pulse Width	t <sub>W</sub>	5		—		—	ns
CP Pulse Width	t <sub>W</sub>	5		—		—	ns
CP Frequency	f <sub>MAX</sub>	5		—		—	MHz

†5 V: min. is @ 4.5 V

5 V: min. is @ 4.75 V for 0 to +70°C

### SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn	t <sub>PLH</sub> t <sub>PHL</sub>	5†	2.5	12.6	2.4	14	ns
MR to Qn	t <sub>PLH</sub> t <sub>PHL</sub>	5	2.6	12.7	2.5	14.2	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—		10		10	pF
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF

†min. is @ 5.5 V

max. is @ 4.5 V

min. is @ 5.25 V for 0 to +70°C

max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per flip-flop.

P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>i</sub> + Σ (C<sub>L</sub> V<sub>CC</sub><sup>2</sup> f<sub>o</sub>) + V<sub>CC</sub> ΔI<sub>CC</sub> where f<sub>i</sub> = input frequency  
f<sub>o</sub> = output frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.

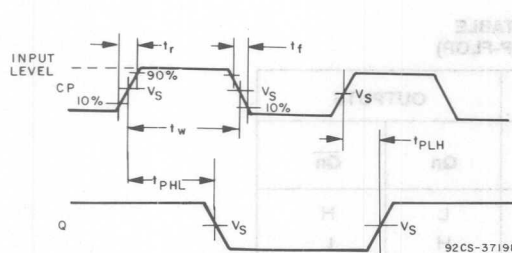


Fig. 1 - Propagation delay times and clock pulse width.

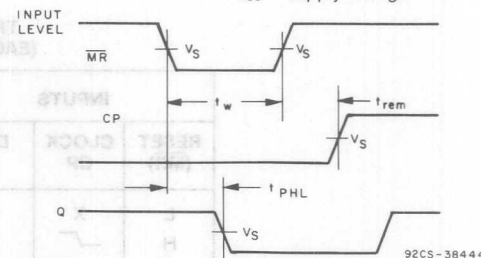


Fig. 2 - Prerequisite and propagation delay times for master reset.

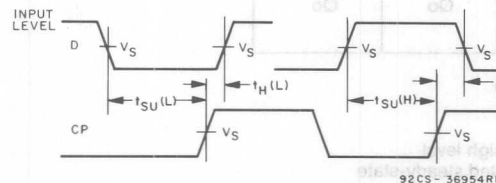
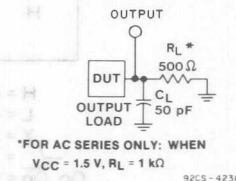


Fig. 3 - Prerequisite for clock.



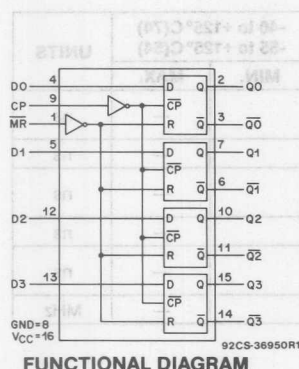
\*FOR AC SERIES ONLY: WHEN  
V<sub>CC</sub> = 1.5 V, R<sub>L</sub> = 1 kΩ

Fig. 4 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V <sub>CC</sub>	3 V
Input Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	1.5 V
Output Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>

# CD54/74AC175 CD54/74ACT175

Product Preview



## Quad D Flip-Flop with Reset

### Type Features:

- Buffered inputs
- Typical propagation delay:  
6.4 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

The RCA CD54/74AC175 and CD54/74ACT175 are quad D flip-flops with reset that utilize RCA's new ADVANCED CMOS LOGIC technology. Information at the D input is transferred to the Q and  $\bar{Q}$  outputs on the positive-going edge of the clock pulse. All four flip-flops are controlled by a common clock (CP) and a common reset (MR). Resetting is accomplished by a LOW logic level independent of the clock.

The CD54AC/ACT175 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT164 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar AST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE  
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
RESET (MR)	CLOCK CP	DATA D <sub>n</sub>	Q <sub>n</sub>	$\bar{Q}_n$
L	X	X	L	H
H		H	H	L
H		L	L	H
H	L	X	Q <sub>0</sub>	$\bar{Q}_0$

H = High level (steady state)  
L = Low level (steady state)  
X = Irrelevant  
 = Transition from low to high level  
Q<sub>0</sub>,  $\bar{Q}_0$  = Levels before the indicated steady-state input conditions were established

CD54/74AC	CD54/74ACT
3 V	3 V
1.5 V	1.5 V
0.5 V	0.5 V

File Number 1964



CD54/74AC175  
CD54/74ACT175

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

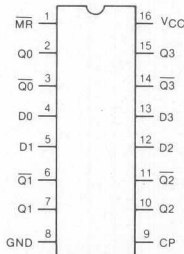
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A =$ Full Package-Temperature Range) AC Types ACT Types	1.5	5.5	V
	4.5	5.5	V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40	$+125$	$^\circ\text{C}$
	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0	50	ns/V
	0	20	ns/V
	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.



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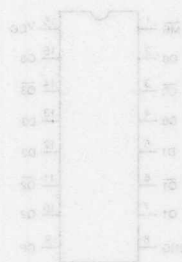
TERMINAL ASSIGNMENT

# STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
	V <sub>I</sub> (V)	I <sub>O</sub> (mA)		+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V <sub>OH</sub>	V <sub>IH</sub>	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
	or	-0.05	3	2.9	—	2.9	—	2.9	—	
	V <sub>IL</sub>	-0.05	4.5	4.4	—	4.4	—	4.4	—	
	#	-4	3	2.58	—	2.48	—	2.4	—	
	*	-24	4.5	3.94	—	3.8	—	3.7	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V <sub>OL</sub>	V <sub>IH</sub>	0.05	1.5	—	0.1	—	0.1	—	0.1	V
	or	0.05	3	—	0.1	—	0.1	—	0.1	
	V <sub>IL</sub>	0.05	4.5	—	0.1	—	0.1	—	0.1	
	#	12	3	—	0.36	—	0.44	—	0.5	
	*	24	4.5	—	0.36	—	0.44	—	0.5	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.



TERMINAL ASSIGNMENT

# CD54/74AC175

## CD54/74ACT175

### STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70		-40 to +125(74)		
							-40 to +85		-55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
Dn	0.58
MR	0.67
CP	0.92

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC175 CD54/74ACT175

## PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t <sub>SU</sub>	1.5 3.3* 5†	—	—	—	—	ns
Hold Time	t <sub>H</sub>	1.5 3.3 5	—	—	—	—	ns
Removal Time MR to CP	t <sub>REM</sub>	1.5 3.3 5	—	—	—	—	ns
MR Pulse Width	t <sub>W</sub>	1.5 3.3 5	—	—	—	—	ns
CP Pulse Width	t <sub>W</sub>	1.5 3.3 5	—	—	—	—	ns
CP Frequency	f <sub>MAX</sub>	1.5 3.3 5	—	—	—	—	MHz

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

5 V: min is @ 4.75 V for 0 to +70°C

## SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q, $\bar{Q}$	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3* 5†	— 3.3 2.2	136 15.3 10.9	— 3.1 2.1	153 17.1 12.2	ns
MR to Q, $\bar{Q}$	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 3.7 2.4	151 16.9 12.1	— 3.5 2.3	169 18.9 13.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	—	—	—	—	pF
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V.  
max. is @ 3 V.

†5 V: min. is @ 5.5 V.  
max. is @ 4.5 V.

min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per flip-flop.

P<sub>D</sub> = C<sub>PD</sub>V<sub>CC</sub><sup>2</sup> f<sub>i</sub> + Σ (C<sub>L</sub>V<sub>CC</sub><sup>2</sup> f<sub>o</sub>) where f<sub>i</sub> = input frequency

f<sub>o</sub> = output frequency

C<sub>L</sub> = output load capacitance

V<sub>CC</sub> = supply voltage.

# CD54/74AC175

## CD54/74ACT175

### PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	$t_{SU}$	5†	—	—	—	—	ns
Hold Time	$t_H$	5	—	—	—	—	ns
Removal Time MR to CP	$t_{REM}$	5	—	—	—	—	ns
MR Pulse Width	$t_W$	5	—	—	—	—	ns
CP Pulse Width	$t_W$	5	—	—	—	—	ns
CP Frequency	$f_{max}$	5	—	—	—	—	MHz

† min. is @ 4.5 V  
min. is @ 4.75 V for 0 to +70°C

### SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3$ ns, $C_L = 50$ pF

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q, $\bar{Q}$	$t_{PLH}$ $t_{PHL}$	5†	2.4	12.1	2.3	13.5	ns
MR to Q, $\bar{Q}$	$t_{PLH}$ $t_{PHL}$	5	2.7	13.3	2.5	14.9	ns
Power Dissipation Capacitance	$C_{PD}$	—	—	—	—	—	pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

† min. is @ 5.5 V  
max. is @ 4.5 V  
min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

$C_{PD}$  is used to determine the dynamic power consumption, per flip-flop.  
 $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_i V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
 $f_o$  = output frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

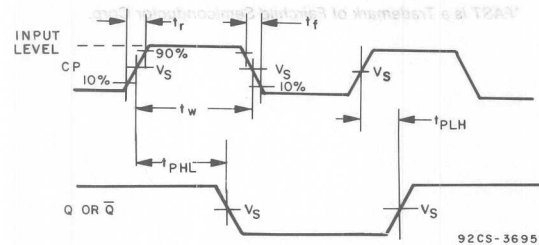


Fig. 1 - Propagation delay times and clock pulse width.

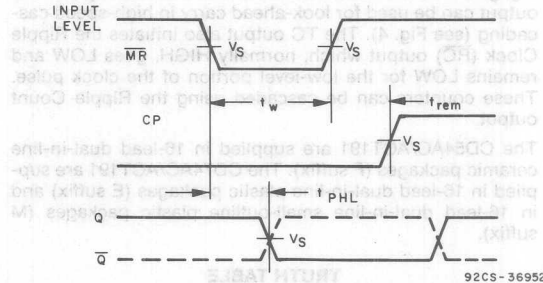


Fig. 2 - Prerequisite and propagation delay times for master reset.

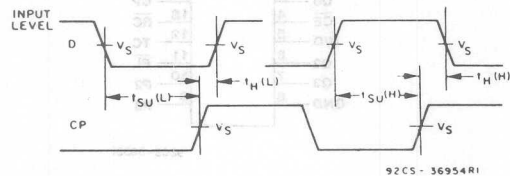
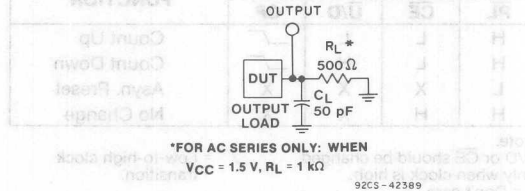


Fig. 3 - Prerequisite for clock.

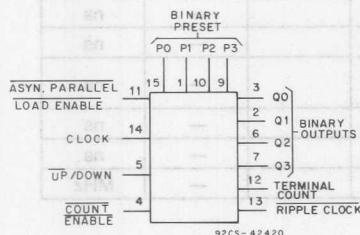


\*FOR AC SERIES ONLY: WHEN  
 $V_{CC} = 1.5$  V,  $R_L = 1$  k $\Omega$

Fig. 4 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$





## Presettable Synchronous 4-Bit Binary Up/Down Counter

### Type Features:

- Buffered inputs
- Typical propagation delay:  
12.8 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

### FUNCTIONAL DIAGRAM

The GE/RCA-CD54/74AC191 and CD54/74ACT191 are asynchronously presettable binary up/down synchronous counters that utilize GE/RCA's new ADVANCED CMOS LOGIC technology. Presetting the counter to the number on preset data inputs (P0-P3) is accomplished by setting LOW the asynchronous parallel load input (PL). Counting occurs when PL is HIGH, Count Enable (CE) is LOW, and the Up/Down (U/D) input is either LOW for up-counting or HIGH for down-counting. The counter is incremented or decremented synchronously with the LOW-to-HIGH transition of the clock.

When an overflow or underflow of the counter occurs, the Terminal Count (TC) output, which is LOW during counting, goes HIGH and remains HIGH for one clock cycle. This output can be used for look-ahead carry in high-speed cascading (see Fig. 4). The TC output also initiates the Ripple Clock (RC) output which, normally HIGH, goes LOW and remains LOW for the low-level portion of the clock pulse. These counters can be cascaded using the Ripple Count output.

The CD54AC/ACT191 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT191 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix).

### TRUTH TABLE

INPUTS				FUNCTION
PL	CE	U/D	CP	
H	L	L		Count Up
H	L	H		Count Down
L	X	X	X	Asyn. Preset
H	H	X	X	No Change

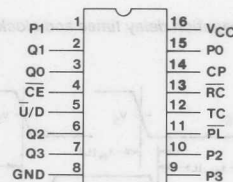
Note:  
U/D or CE should be changed only when clock is high.  
X = Don't care.

= Low-to-high clock transition.

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.



### TERMINAL ASSIGNMENT

# CD54/74AC191

## CD54/74ACT191

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\* (For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *, (For $T_A =$ Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I, V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	+125	$^\circ\text{C}$
CD54 Types	-55	+125	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\* Unless otherwise specified, all voltages are referenced to ground.

# CD54/74AC191 CD54/74ACT191

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
						+25		0 to +70		-40 to +125(74)		
								-40 to +85		-55 to +125(54)		
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V <sub>IH</sub>					1.5	1.2	—	1.2	—	1.2	—	V
					3	2.1	—	2.1	—	2.1	—	
					5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V <sub>IL</sub>					1.5	—	0.3	—	0.3	—	0.3	V
					3	—	0.9	—	0.9	—	0.9	
					5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V <sub>OH</sub>			V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
				-0.05	3	2.9	—	2.9	—	2.9	—	
				-0.05	4.5	4.4	—	4.4	—	4.4	—	
				-4	3	2.58	—	2.48	—	2.4	—	
				-24	4.5	3.94	—	3.8	—	3.7	—	
				-75	5.5	—	—	3.85	—	—	—	
				-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V <sub>OL</sub>			V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
				0.05	3	—	0.1	—	0.1	—	0.1	
				0.05	4.5	—	0.1	—	0.1	—	0.1	
				12	3	—	0.36	—	0.44	—	0.5	
				24	4.5	—	0.36	—	0.44	—	0.5	
				75	5.5	—	—	—	1.65	—	—	
				50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I <sub>I</sub>			V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I <sub>CC</sub>			V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# CD54/74AC191

## CD54/74ACT191

### STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
P0 — P3, PL	0.75
CL, U/D, CE	0.85

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f <sub>max</sub> †	1.5 3.3* 5†	5 35 65	— — —	4.4 30 60	— — —	MHz
CP Pulse Width	t <sub>w</sub>	1.5 3.3 5	100 14.3 7.6	— — —	115 16 8.3	— — —	ns
PL Pulse Width	t <sub>w</sub>	1.5 3.3 5	73 10.2 5.5	— — —	88 12.3 6	— — —	ns
Recovery Time	t <sub>REC</sub>	1.5 3.3 5	73 10.2 6	— — —	88 12.3 6.5	— — —	ns
Setup Time: Pn to PL	t <sub>su</sub>	1.5 3.3 5	50 7 3.7	— — —	53 7.6 4	— — —	ns
CE to CP	t <sub>su</sub>	1.5 3.3 5	130 18 9.7	— — —	140 20 10.5	— — —	ns
U/D to CP	t <sub>su</sub>	1.5 3.3 5	145 20 11	— — —	160 23 12	— — —	ns
Hold Time: Pn to PL	t <sub>h</sub>	1.5 3.3 5	30 4.2 2	— — —	33 4.8 2	— — —	ns
CE to CP	t <sub>h</sub>	1.5 3.3 5	0 0 0	— — —	0 0 0	— — —	ns
U/D to CP	t <sub>h</sub>	1.5 3.3 5	0 0 0	— — —	0 0 0	— — —	ns

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

5 V: min is @ 4.75 V for 0 to +70°C

‡Applies to non-cascaded operation only. With cascaded counters clock-to-terminal count propagation delays, count enable (CE)-to-clock set-up times, and count enable (CE)-to-clock hold times determine max. clock frequency. For example, with these AC devices @ 85°C and V<sub>CC</sub> = 5 V:

$$f_{\max}(\text{CP}) = \frac{1}{\text{CP-to-TC prop. delay} + \text{CE-to-CP setup} + \text{CE-to-CP Hold}} = \frac{1}{18.7 + 9.7 + 0} \approx 35 \text{ MHz}$$



# CD54/74AC191

## CD54/74ACT191

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ 

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
PL to Qn	$t_{PLH}$	1.5	—	180	—	200	ns
	$t_{PHL}$	3.3*	4.5	19.3	4.3	21	ns
		5†	2.8	13.8	2.6	15	ns
Pn to Qn	$t_{PLH}$	1.5	—	185	—	205	ns
	$t_{PHL}$	3.3	4.4	19.6	4.3	21.3	ns
		5	2.8	14	2.6	15.2	ns
CP to Qn	$t_{PLH}$	1.5	—	195	—	215	ns
	$t_{PHL}$	3.3	4.7	20.7	4.4	22.4	ns
		5	3	14.8	2.7	16	ns
CP to $\overline{RC}$	$t_{PLH}$	1.5	—	145	—	160	ns
	$t_{PHL}$	3.3	3.5	15.4	3.4	16.8	ns
		5	2.2	11	2.1	12	ns
CP to TC	$t_{PLH}$	1.5	—	245	—	270	ns
	$t_{PHL}$	3.3	6	26.2	5.5	28	ns
		5	3.8	18.7	3.4	20	ns
$\overline{U/D}$ to $\overline{RC}$	$t_{PLH}$	1.5	—	265	—	295	ns
	$t_{PHL}$	3.3	6.5	28	6.1	30.4	ns
		5	4.1	20	3.7	21.7	ns
$\overline{U/D}$ to TC	$t_{PLH}$	1.5	—	170	—	190	ns
	$t_{PHL}$	3.3	4.2	18.2	4	19.7	ns
		5	2.6	13	2.4	14.1	ns
$\overline{CE}$ to $\overline{RC}$	$t_{PLH}$	1.5	—	150	—	165	ns
	$t_{PHL}$	3.3	3.6	15.5	3.4	16.9	ns
		5	2.2	11.1	2.1	12.1	ns
Power Dissipation Capacitance	$C_{PD}\S$	—	96 Typ.		96 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§ $C_{PD}$  is used to determine the dynamic power consumption, per package.

$PD = C_{PD} V_{CC}^2 f_i + (C_L V_{CC}^2 f_o)$  where  
 $f_i$  = input frequency  
 $f_o$  = output frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

# Technical Data

## CD54/74AC191 CD54/74ACT191

### PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f <sub>max</sub> †	5*	65	—	60	—	MHz
CP Pulse Width	t <sub>w</sub>	5	7.6	—	8.3	—	ns
PL Pulse Width	t <sub>w</sub>	5	5.5	—	6	—	ns
Recovery Time	t <sub>REC</sub>	5	6	—	6.5	—	ns
Setup Time: Pn to PL	t <sub>SU</sub>	5	3.7	—	4	—	ns
CE to CP		5	9.7	—	10.5	—	
U/D to CP		5	11	—	12	—	
Hold Time: Pn to PL	t <sub>H</sub>	5	2	—	2	—	ns
CE to CP		5	0	—	0	—	
U/D to CP		5	0	—	0	—	

\*min. is @ 4.5 V

min. is @ 4.75 V for 0 to +70°C

†Applies to non-cascaded operation only. With cascaded counters clock-to-terminal count propagation delays, count enable (CE)-to-clock set-up times, and count enable (CE)-to-clock hold times determine max. clock frequency. For example, with these ACT devices @ 85°C:

$$f_{\max}(\text{CP}) = \frac{1}{\text{CP-to-TC prop. delay} + \text{CE-to-CP setup} + \text{CE-to-CP Hold}} = \frac{1}{18.7 + 9.7 + 0} \approx 35 \text{ MHz}$$

### SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:	t <sub>PLH</sub> t <sub>PHL</sub>	5*	3	15	2.8	16.3	ns
PL to Qn		5	2.8	14	2.6	15.2	
Pn to Qn		5	3	14.8	2.7	16	
CP to Qn		5	2.2	11	2.1	12	
CP to RC		5	3.8	18.7	3.4	20	
CP to TC		5	4.1	20	3.7	21.7	
U/D to RC		5	2.8	13.7	2.6	14.9	
U/D to TC		5	2.4	11.7	2.2	12.7	
CE to RC							
Power Dissipation Capacitance	C <sub>PD</sub> †	—	133 Typ.		133 Typ.		pF
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF

\*Min. is @ 5.5 V

Max. is @ 4.5 V.

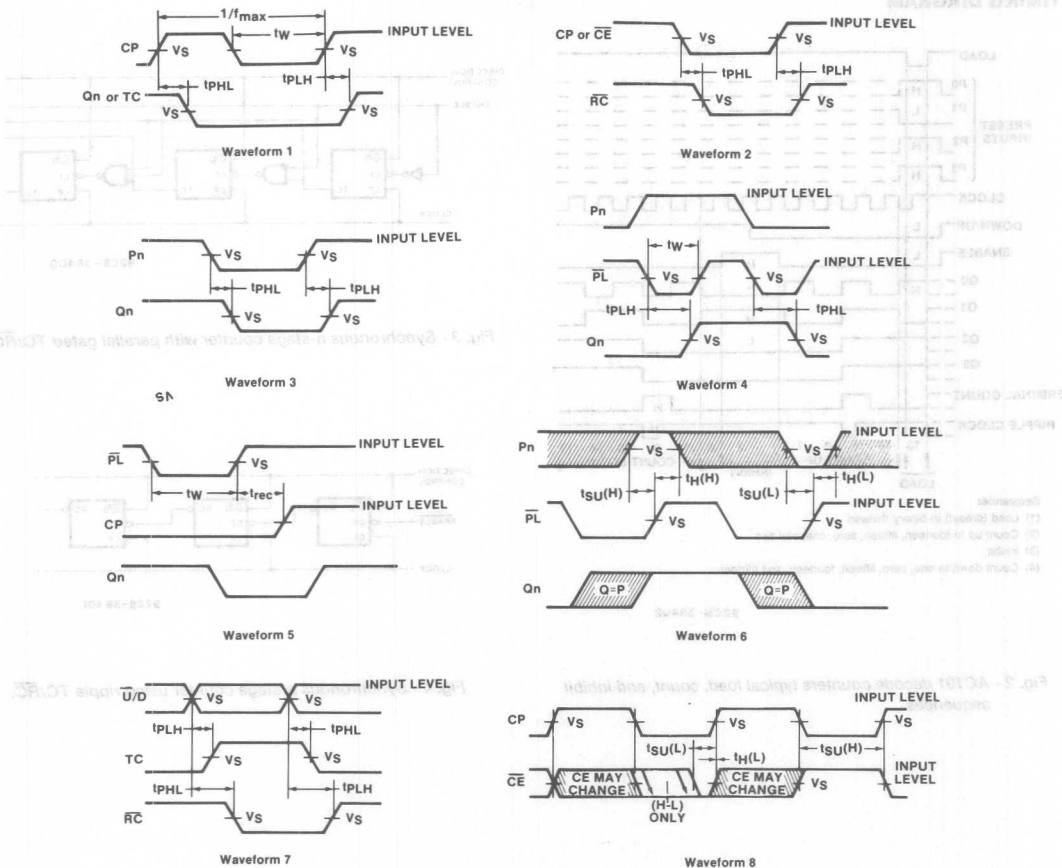
Min. is @ 5.25 V for 0 to +70°C

Max. is @ 4.75 V for 0 to +70°C

†C<sub>PD</sub> is used to determine the dynamic power consumption, per package.

PD = C<sub>PD</sub>V<sub>CC</sub><sup>2</sup> f<sub>i</sub> + (C<sub>L</sub>V<sub>CC</sub><sup>2</sup> f<sub>o</sub>) + V<sub>CC</sub> ΔI<sub>CC</sub> where  
f<sub>i</sub> = input frequency  
f<sub>o</sub> = output frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.

Technical Data  
**CD54/74AC191**  
**CD54/74ACT191**



The shaded areas indicate when the input is permitted to change for predictable output performance

92CL-38403R3

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$

Fig. 1 - Transition, propagation delay, setup and hold, and removal times.

## TIMING DIAGRAM

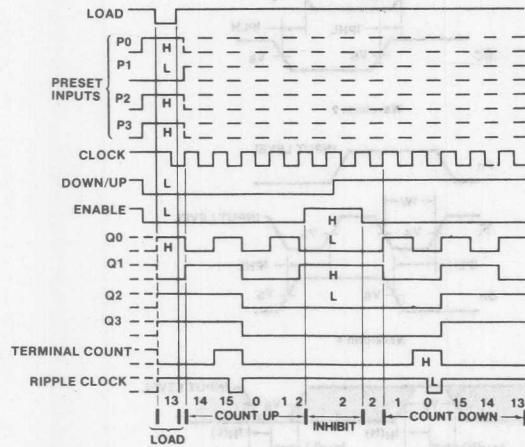


Fig. 2 - AC191 decode counters typical load, count, and inhibit sequences.

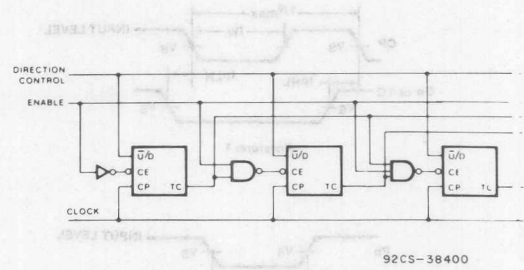


Fig. 3 - Synchronous n-stage counter with parallel gated TC/RC.

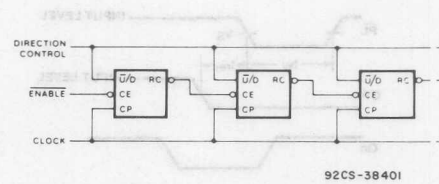
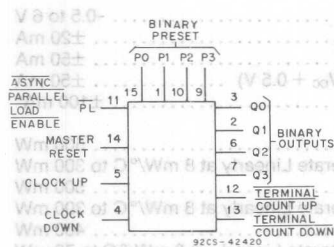


Fig. 4 - Synchronous n-stage counter using ripple TC/RC.

Output Switching Voltage, $V_o$	Input Switching Voltage, $V_i$	Input Level
0.8 V <sub>cc</sub>	0.8 V <sub>cc</sub>	0.8 V <sub>cc</sub>
0.8 V <sub>cc</sub>	0.8 V <sub>cc</sub>	0.8 V <sub>cc</sub>
0.8 V <sub>cc</sub>	0.8 V <sub>cc</sub>	0.8 V <sub>cc</sub>

# CD54/74AC193

## CD54/74ACT193



### FUNCTIONAL DIAGRAM

The GE/RCA-CD54/74AC193 and CD54/74ACT193 are up/down binary counters with separate up/down clocks. These devices utilize GE/RCA's new ADVANCED CMOS LOGIC technology. Presetting the counter to the number on preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input ( $\overline{PL}$ ). The counter is incremented on the LOW-to-HIGH transition of the Clock-Up input (and a HIGH level on the Clock-Down input) and decremented on the LOW-to-HIGH transition of the Clock-Down input (and a HIGH level on the Clock-Up input). A HIGH level on the Reset input overrides any other input to clear the counter to its zero state. The TCU (carry) output goes LOW half a clock period before the zero count is reached and returns to a HIGH level at the zero count. The TCD (borrow) output in the count down mode likewise goes LOW half a clock period before the maximum count (15 counts) and returns to HIGH at the maximum count. Cascading is effected by connecting the TCU and TCD outputs of a less significant counter to the Clock-Up and Clock-Down inputs, respectively, of the next most significant counter.

The CD54AC/ACT193 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT193 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix).

### TRUTH TABLE

CLOCK UP	CLOCK DOWN	RESET	PARALLEL LOAD	FUNCTION
	H	L	H	Count Up
H		L	H	Count Down
X	X	H	X	Reset
X	X	L	L	Load Preset Inputs

H = High level

L = Low level

= Low-to-high transition

X = Don't care

## Presetable Synchronous 4-Bit Binary Up/Down Counter with Reset

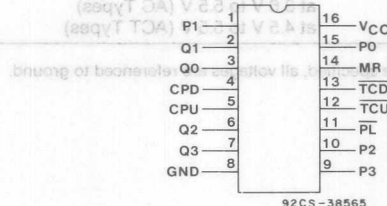
### Type Features:

- Buffered inputs
- Typical propagation delay: 11.2 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.



### TERMINAL ASSIGNMENT



# CD54/74AC193 CD54/74ACT193

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

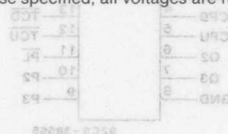
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.



TERMINAL ASSIGNMENT

FUNCTION	PARALLEL LOAD	RESET	CLOCK DOWN	CLOCK UP
Count Up	H	L	H	
Count Down	H	L		H
Reset	X	H	X	X
Load Preset	L	L	X	X

H = High level  
L = Low level  
X = Low-to-high transition  
= Don't care

**CD54/74AC193**  
**CD54/74ACT193**

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

## CD54/74AC193

## CD54/74ACT193

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
P0 - P3, PL	0.75
MR, CPU, CPD	0.85

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC193

## CD54/74ACT193

## PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS	
			MIN.	MAX.	MIN.	MAX.		
Clock Pulse Width CPD	t <sub>w</sub>	1.5	72	—	85	—	ns	
		3.3*	10.6	—	11.9	—		
		5†	5.5	—	5.8	—		
CPU	t <sub>w</sub>	1.5	83	—	95	—	ns	
		3.3	12	—	13.2	—		
		5	6.2	—	6.6	—		
PL Pulse Width	t <sub>w</sub>	1.5	72	—	88	—	ns	
		3.3	10.6	—	12.3	—		
		5	5.5	—	6	—		
MR Pulse Width	t <sub>w</sub>	1.5	60	—	67	—	ns	
		3.3	8.5	—	9.5	—		
		5	4.6	—	5	—		
Recovery Time PL to CPU or CPD	t <sub>REC</sub>	1.5	60	—	67	—	ns	
		3.3	8.5	—	9.5	—		
		5	4.6	—	5	—		
Recovery Time MR to CPU, CPD	t <sub>REC</sub>	1.5	1	—	1	—	ns	
		3.3	1	—	1	—		
		5	1	—	1	—		
Setup Time P <sub>n</sub> to PL	t <sub>SU</sub>	1.5	48	—	54	—	ns	
		3.3	6.8	—	7.6	—		
		5	3.7	—	4	—		
Hold Time P <sub>n</sub> to PL	t <sub>H</sub>	1.5	2	—	2	—	ns	
		3.3	2	—	2	—		
		5	2	—	2	—		
Max. Frequency CPU	f <sub>max</sub>	1.5	6	—	5.3	—	MHz	
		3.3	42	—	38	—		
		5	80	—	75	—		
CPD			1.5	7	—	5.9	—	MHz
			3.3	47	—	42	—	
			5	90	—	85	—	

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

5 V: min. is @ 4.75 V for 0 to +70°C



# CD54/74AC193

## CD54/74ACT193

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ 

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C (74) -55 to +125°C (54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: PL to Qn	$t_{PLH}$	1.5	—	180	—	200	ns
	$t_{PHL}$	3.3*	4.5	19.3	4.3	21	
		5†	2.8	13.8	2.6	15	
CPU to Qn CPD to Qn	$t_{PLH}$	1.5	—	170	—	188	ns
	$t_{PHL}$	3.3	4.2	18.1	4	19.6	
		5	2.7	12.9	2.4	14	
CPU to $\overline{TCU}$ CPD to $\overline{TCD}$	$t_{PLH}$	1.5	—	135	—	152	ns
	$t_{PHL}$	3.3	3.3	14.4	3.2	15.7	
		5	2.1	10.3	1.9	11.2	
MR to Qn	$t_{PLH}$	1.5	—	195	—	215	ns
	$t_{PHL}$	3.3	4.7	20.6	4.4	22.4	
		5	3	14.7	2.7	16	
MR to $\overline{TCU}$	$t_{PLH}$	1.5	—	180	—	200	ns
	$t_{PHL}$	3.3	4.5	19.3	4.3	21	
		5	2.8	13.8	2.6	15	
MR to $\overline{TCD}$	$t_{PLH}$	1.5	—	218	—	245	ns
	$t_{PHL}$	3.3	5.4	23.8	5.2	25.5	
		5	3.4	17	3.1	18.2	
Pn to Qn	$t_{PLH}$	1.5	—	200	—	222	ns
	$t_{PHL}$	3.3	4.9	21.3	4.6	23.1	
		5	3.1	15.2	2.8	16.5	
Power Dissipation Capacitance	$C_{PD}^\ddagger$	—	95 Typ.		95 Typ.		pF
Input Capacitance	$C_I$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

‡ $C_{PD}$  is used to determine the dynamic power consumption, per package.

$PD = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$  where  $f_i$  = input frequency  
 $f_o$  = output frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.



## PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width: CPU	$t_w$	5*	7.1	—	7.7	—	ns
CPD			6.2	—	6.6	—	
PL Pulse Width	$t_w$	5	6.9	—	7.5	—	ns
MR Pulse Width	$t_w$	5	4.6	—	5	—	ns
Recovery Time: PL to CPU or CPD	$t_{REC}$	5	6	—	6.5	—	ns
MR to CPU, CPD			1	—	1	—	
Setup Time Pn to $\overline{PL}$	$t_{SU}$	5	5	—	5.4	—	ns
Hold Time Pn to $\overline{PL}$	$t_H$	5	2	—	2	—	ns
Max. Frequency: CPU	$f_{max}$	5	70	—	65	—	MHz
CPD			80	—	75	—	

\*5V min. is @ 4.5 V

5V: min. is @ 4.75 V for 0 to +70°C

SWITCHING CHARACTERISTICS: ACT Series;  $t_r = 3$  ns,  $C_L = 50$  pF

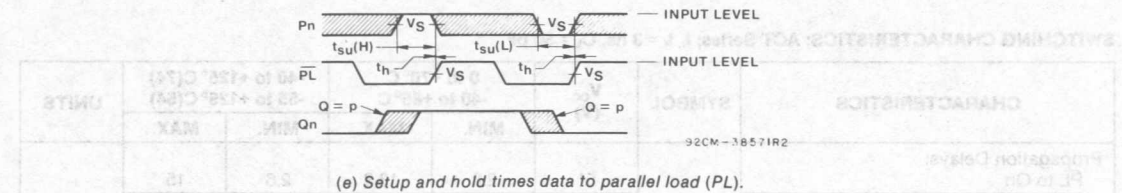
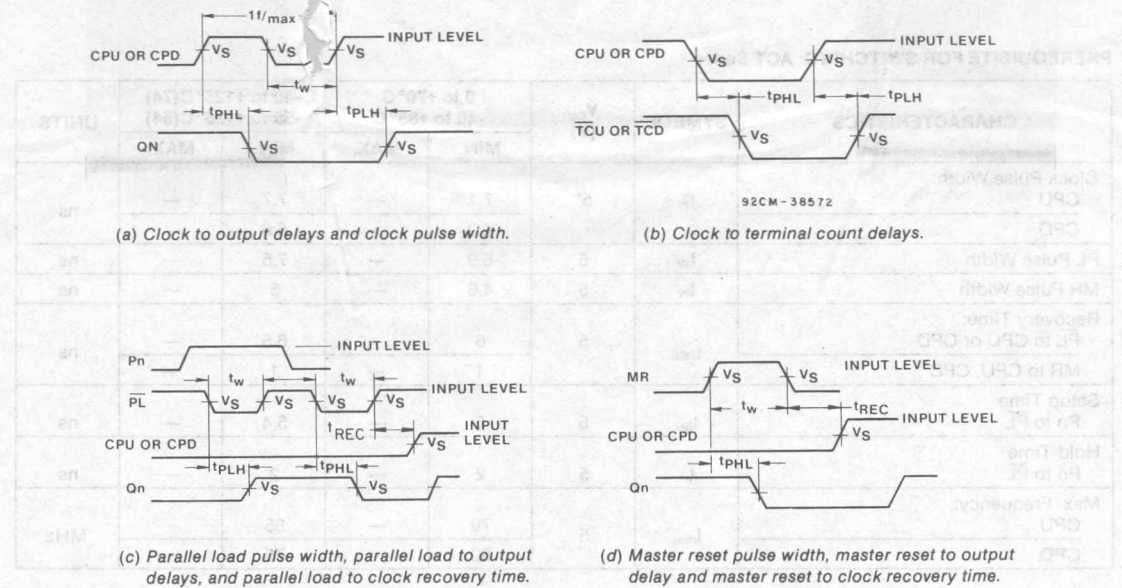
CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: PL to Qn	$t_{PLH}$ $t_{PHL}$	5*	2.8	13.8	2.6	15	ns
CPU to Qn		5	2.7	12.9	2.4	14	
CPD to Qn		5	2.7	12.9	2.4	14	
CPU to $\overline{TCU}$		5	2.1	10.3	1.9	11.2	
CPD to $\overline{TCU}$		5	2.1	10.3	1.9	11.2	
MR to Qn		5	3	14.7	2.7	16	
MR to $\overline{TCU}$		5	2.8	13.8	2.6	15	
MR to $\overline{TCU}$		5	3.4	17	3.1	18.2	
Pn to Qn		5	3.1	15.2	2.8	16.5	
Power Dissipation Capacitance	$C_{PD}^\dagger$	—	126 Typ.		126 Typ.		pF
Input Capacitance	$C_I$	—	—	10	—	10	pF

\*5V: min. is @ 5.5 V

max. is @ 4.5 V

5V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C $^\dagger C_{PD}$  is used to determine the dynamic power consumption, per package.
 $PD = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ , where  $f_i$  = input frequency  
 $f_o$  = output frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

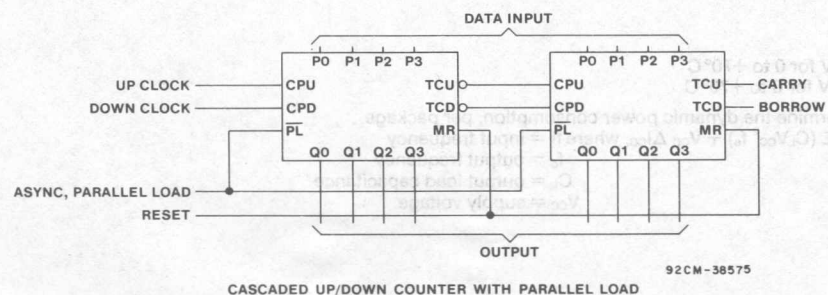
# CD54/74AC193 CD54/74ACT193



	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$

Fig. 1 - AC waveforms.

## APPLICATION



# CD54/74AC193 CD54/74ACT193

## Sequences:

- (1) Reset outputs to zero.
- (2) Load (preset) to binary thirteen.
- (3) Count up to fourteen, fifteen, terminal count up, zero, one and two.
- (4) Count down to one, zero, terminal count down, fifteen, fourteen and thirteen.

Note 1: Master reset overrides load data and clock inputs

Note 2: When counting up, clock-down input must be high; when counting down, clock-up input must be high.

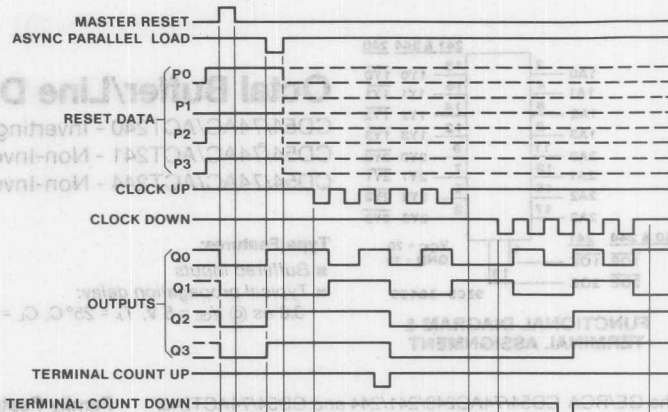


Fig. 2 - Timing diagram.

TRUTH TABLES		
OUTPUT	INPUTS	
Y	A	10E 30E
L	L	L
H	H	L
Z	X	H

(AC/ACT193)

TRUTH TABLES		
OUTPUT	INPUTS	
Y	A	10E 30E
L	L	L
H	H	L
Z	X	H

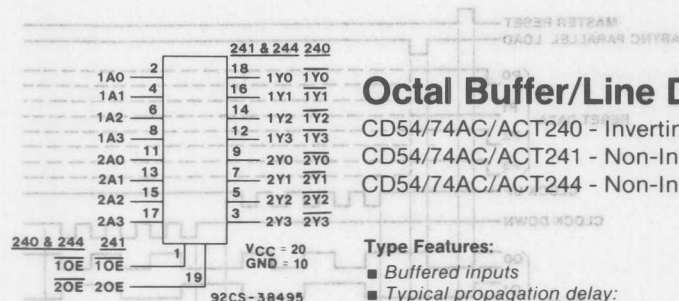
(AC/ACT193)

TRUTH TABLES					
OUTPUT		INPUTS		INPUTS	
ZY	ZA	Y	30E	1A	10E
L	X	L	L	L	L
L	L	H	L	L	L
L	H	Z	H	X	H

(AC/ACT193)

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Indeterminate  
Z = HIGH Impedance

# CD54/74AC240/241/244 CD54/74ACT240/241/244



## Octal Buffer/Line Drivers, 3-State

CD54/74AC/ACT240 - Inverting  
CD54/74AC/ACT241 - Non-Inverting  
CD54/74AC/ACT244 - Non-Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay:  
3.6 ns @  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50 pF$

### FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

The GE/RCA CD54/74AC240/241/244 and CD54/74ACT240/241/244 are 3-state octal buffer/line drivers that utilize GE/RCA's new ADVANCED CMOS LOGIC technology. The CD54/74AC/ACT240 and CD54/74AC/ACT244 have active-LOW output enables ( $\overline{10E}$ ,  $\overline{20E}$ ). The CD54/74AC/ACT241 has one active-LOW ( $\overline{10E}$ ) and one active-HIGH ( $\overline{20E}$ ) output enable.

The CD54AC240/241/244 and CD54ACT240/241/244 are supplied in 20-lead dual-in-line ceramic packages (F suffix). The CD74AC240/241/244 and CD74ACT240/241/244 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST<sup>®</sup>/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24$ -mA output drive current
  - Fanout to 15 FAST<sup>®</sup> ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

### TRUTH TABLES

INPUTS		OUTPUT	
$\overline{10E}$ , $\overline{20E}$	A	Y	
L	L	H	
L	H	L	
H	X	Z	

(AC/ACT240)

INPUTS		OUTPUT	
$\overline{10E}$ , $\overline{20E}$	A	Y	
L	L	L	
L	H	H	
H	X	Z	

(AC/ACT244)

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{10E}$	1A	1Y	$\overline{20E}$	2A	2Y
L	L	L	L	X	Z
L	H	H	H	L	L
H	X	Z	H	H	H

(AC/ACT241)

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = HIGH Impedance

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*

**POWER DISSIPATION PER PACKAGE ( $P_D$ ):**

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at $8\text{ mW}/^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at $8\text{ mW}/^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at $6\text{ mW}/^\circ\text{C}$ to 70 mW

**OPERATING-TEMPERATURE RANGE ( $T_A$ ):**

PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$

**STORAGE TEMPERATURE ( $T_{stg}$ )**

LEAD TEMPERATURE (DURING SOLDERING):	-65 to $+150^\circ\text{C}$
--------------------------------------	-----------------------------

At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

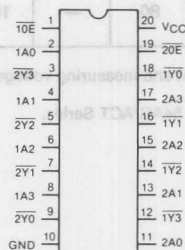
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

**RECOMMENDED OPERATING CONDITIONS:**

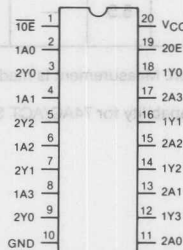
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ ; (For $T_A =$ Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40 -55	$+125$ $+125$	$^\circ\text{C}$ $^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

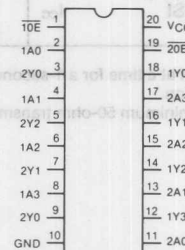
\*Unless otherwise specified, all voltages are referenced to ground.



**CD54/74AC, ACT240 TYPES  
TERMINAL ASSIGNMENT**



**CD54/74AC, ACT241 TYPES  
TERMINAL ASSIGNMENT**



**CD54/74AC, ACT244 TYPES  
TERMINAL ASSIGNMENT**



# CD54/74AC240/241/244

## CD54/74ACT240/241/244

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
						+25		0 to +70		-40 to +125(74)			
								-40 to +85		-55 to +125(54)			
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage V <sub>IH</sub>					1.5	1.2	—	1.2	—	1.2	—	V	
					3	2.1	—	2.1	—	2.1	—		
					5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage V <sub>IL</sub>					1.5	—	0.3	—	0.3	—	0.3	V	
					3	—	0.9	—	0.9	—	0.9		
					5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage V <sub>OH</sub>			V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V	
				-0.05	3	2.9	—	2.9	—	2.9	—		
				-0.05	4.5	4.4	—	4.4	—	4.4	—		
				-4	3	2.58	—	2.48	—	2.4	—		
				-24	4.5	3.94	—	3.8	—	3.7	—		
				-75	5.5	—	—	3.85	—	—	—		
				-50	5.5	—	—	—	—	3.85	—		
Low-Level Output Voltage V <sub>OL</sub>			V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V	
				0.05	3	—	0.1	—	0.1	—	0.1		
				0.05	4.5	—	0.1	—	0.1	—	0.1		
				12	3	—	0.36	—	0.44	—	0.5		
				24	4.5	—	0.36	—	0.44	—	0.5		
				75	5.5	—	—	1.65	—	—	—		
				50	5.5	—	—	—	—	—	1.65		
Input Leakage Current			V <sub>CC</sub> or GND	I <sub>I</sub>	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current			V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub>	I <sub>OZ</sub>	5.5	—	±0.5	—	±5	—	±10	μA	
			or GND										
Quiescent Supply Current, MSI			V <sub>CC</sub> or GND	I <sub>CC</sub>	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# CD54/74AC240/241/244 CD54/74ACT240/241/244

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
	V <sub>I</sub> (V)	I <sub>O</sub> (mA)		+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V <sub>IH</sub>		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V <sub>IL</sub>		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		#	-24	4.5	3.94	—	3.8	—	3.7	—	
		*	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		#	24	4.5	—	0.36	—	0.44	—	0.5	
		*	75	5.5	—	—	—	1.65	—	—	
		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	µA	
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>		—	—	—	—	—	—	—	
		V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	±0.5	—	±5	—	±10	µA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

## ACT INPUT LOADING TABLES

CD54/74ACT240	
INPUT	UNIT LOADS*
nA0 - A3	1.42
10E	0.83
20E	0.83

CD54/74ACT241	
INPUT	UNIT LOADS*
nA0 - A3	0.5
10E	0.83
20E	1.67

CD54/74ACT244	
INPUT	UNIT LOADS*
nA0 - A3	0.5
10E	0.83
20E	0.83

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

**SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$** 

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Outputs AC240	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3* 5†	— 2.2 1.3	85 9.5 6.8	— 2.1 1.3	95 10.6 7.6	ns
AC241, 244	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 3.9 2.5	108 12 8.6	— 3.8 2.4	120 13.4 9.6	ns
Output Enable and Disable Times	t <sub>PLZ</sub> t <sub>PZL</sub> t <sub>PZH</sub> t <sub>PHZ</sub>	1.5 3.3 5	— 3.9 2.5	150 18 12	— 3.8 2.4	167 20.1 13.4	ns
Power Dissipation Capacitance AC240, 241 AC244	C <sub>PD</sub> §	— —	95 Typ. 80 Typ.		95 Typ. 80 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

**SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$** 

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Outputs ACT240	t <sub>PLH</sub> t <sub>PHL</sub>	5†	1.6	7.8	1.5	8.6	ns
ACT241, 244	t <sub>PLH</sub> t <sub>PHL</sub>	5	1.9	9.6	1.8	10.6	ns
Output Enable and Disable Times	t <sub>PLZ</sub> t <sub>PZL</sub> t <sub>PZH</sub> t <sub>PHZ</sub>	5	2.6	13	2.5	14.4	ns
Power Dissipation Capacitance ACT240, 241 ACT244	C <sub>PD</sub> §	—	115 Typ. 95 Typ.		115 Typ. 95 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>i</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>o</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§ $C_{PD}$  is used to determine the dynamic power consumption, per package.

For AC series:  $PD = V_{CC}^2 f_i (C_{PD} + C_L)$

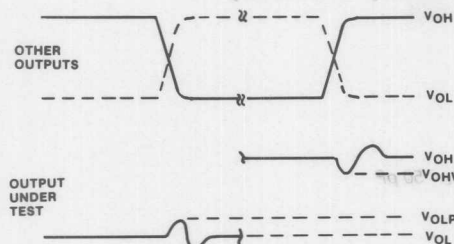
For ACT series:  $PD = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where

$f_i$  = input frequency

$C_L$  = output load capacitance

$V_{CC}$  = supply voltage.

# PARAMETER MEASUREMENT INFORMATION

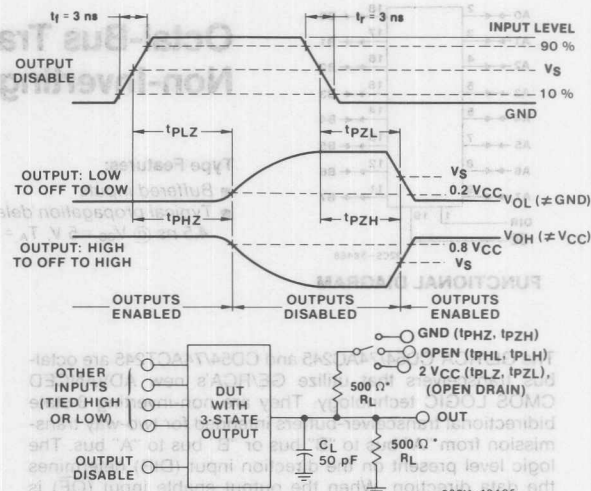


## NOTES:

1.  $V_{OHV}$  AND  $V_{OLP}$  ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:  
PRR  $\leq 1$  MHz,  $t_r = 3$  ns,  $t_f = 3$  ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.  
IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1  $\mu$ F CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

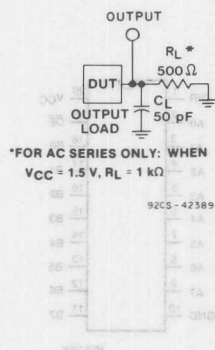
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Fig. 1 - Simultaneous switching transient waveforms.



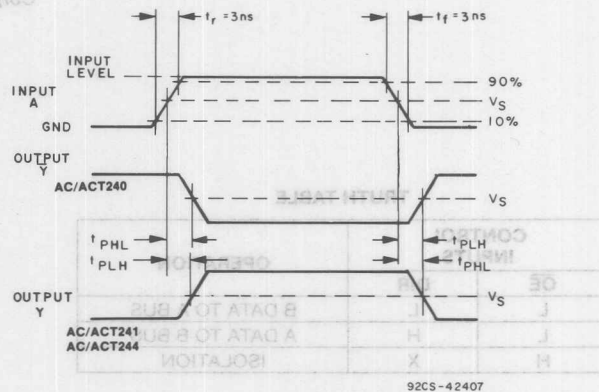
\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5$  V,  $R_L = 1$  k $\Omega$

Fig. 2 - Three-state propagation delay times and test circuit.



\*FOR AC SERIES ONLY: WHEN  
 $V_{CC} = 1.5$  V,  $R_L = 1$  k $\Omega$

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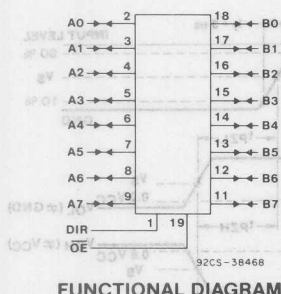
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Fig. 3 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$

# CD54/74AC245 CD54/74ACT245

Advance Information



## Octal-Bus Transceiver, 3-State, Non-Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay:  
4.5 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{ C}$ ,  $C_L = 50\text{ pF}$



The GE/RCA CD54/74AC245 and CD54/74ACT245 are octal-bus transceivers that utilize GE/RCA's new, ADVANCED CMOS LOGIC technology. They are non-inverting 3-state bidirectional transceiver-buffers intended for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus. The logic level present on the direction input (DIR) determines the data direction. When the output enable input (OE) is HIGH, the outputs are in the high-impedance state.

The CD54AC245 and CD54ACT245 are supplied in 20-lead dual-in-line ceramic packages (F suffix). The CD74AC245 and CD74ACT245 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST<sup>®</sup>/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST<sup>®</sup> ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

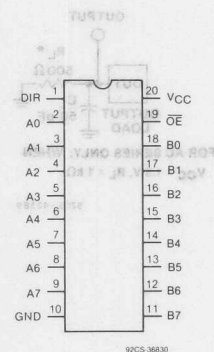


TRUTH TABLE

CONTROL INPUTS		OPERATION
OE	DIR	
L	L	B DATA TO A BUS
L	H	A DATA TO B BUS
H	X	ISOLATION

H = high level, L = low level, X = irrelevant

To prevent excess currents in the High-Z (isolation) modes all I/O terminals should be terminated with 10KΩ to 1MΩ resistors.



### TERMINAL ASSIGNMENT

Input Level	Input Switching Voltage, $V_{IS}$	Output Switching Voltage, $V_{OS}$
3 V	3.0 V	3.0 V
5 V	5.0 V	5.0 V

File Number 1907



# CD54/74AC245 CD54/74ACT245

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

V	CHARACTERISTIC		LIMITS		UNITS
	MIN.	MAX.			
Supply-Voltage Range, $V_{CC}$ *, (For $T_A$ = Full Package-Temperature Range)					
	AC Types	1.5	5.5	V	
	ACT Types	4.5	5.5	V	
DC Input or Output Voltage, $V_I$ , $V_O$					
		0	$V_{CC}$	V	
Operating Temperature, $T_A$ :					
	CD74 Types	-40	+125	°C	
	CD54 Types	-55	+125	°C	
Input Rise and Fall Slew Rate, $dt/dv$					
	at 1.5 V to 3 V(AC Types)	0	50	ns/V	
	at 3.6 V to 5.5 V(AC Types)	0	20	ns/V	
	at 4.5 V to 5.5 V(ACT Types)	0	10	ns/V	

\*Unless otherwise specified, all voltages are referenced to ground.

# STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
						+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)			
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V <sub>IH</sub>		1.5	1.2	—	1.2	—	1.2	—	V			
			3	2.1	—	2.1	—	2.1	—				
			5.5	3.85	—	3.85	—	3.85	—				
Low-Level Input Voltage	V <sub>IL</sub>		1.5	—	0.3	—	0.3	—	0.3	V			
			3	—	0.9	—	0.9	—	0.9				
			5.5	—	1.65	—	1.65	—	1.65				
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V		
			-0.05	3	2.9	—	2.9	—	2.9	—			
			-0.05	4.5	4.4	—	4.4	—	4.4	—			
			-4	3	2.58	—	2.48	—	2.4	—			
			-24	4.5	3.94	—	3.8	—	3.7	—			
			-75	5.5	—	—	3.85	—	—	—			
			-50	5.5	—	—	—	—	3.85	—			
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V		
			0.05	3	—	0.1	—	0.1	—	0.1			
			0.05	4.5	—	0.1	—	0.1	—	0.1			
			12	3	—	0.36	—	0.44	—	0.5			
			24	4.5	—	0.36	—	0.44	—	0.5			
			75	5.5	—	—	—	1.65	—	—			
			50	5.5	—	—	—	—	—	1.65			
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA			
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>											
		V <sub>O</sub> = V <sub>CC</sub>	5.5	—	±0.5	—	±5	—	±10	μA			
Quiescent Supply Current, MSI			I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS	
			+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	$V_{IH}$	4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	$V_{IL}$	4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	4.5	4.4	—	4.4	—	4.4	—
		#	-24	4.5	3.94	—	3.8	—	3.7	—
		*	-75	5.5	—	—	3.85	—	—	—
		*	-50	5.5	—	—	—	—	3.85	—
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.05	4.5	—	0.1	—	0.1	—	0.1
		#	24	4.5	—	0.36	—	0.44	—	0.5
		*	75	5.5	—	—	1.65	—	—	—
		*	50	5.5	—	—	—	—	—	1.65
Input Leakage Current	$I_i$	$V_{CC}$ or GND	5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	$I_{OZ}$	$V_{IH}$ or $V_{IL}$	5.5	—	±0.5	—	±5	—	±10	μA
		$V_O = V_{CC}$ or GND	5.5	—	—	—	—	—	—	—
		$V_{CC}$ or GND	5.5	—	—	—	—	—	—	—
		$V_{CC}$ or GND	5.5	—	—	—	—	—	—	—
Quiescent Supply Current, MSI	$I_{CC}$	$V_{CC}$ or GND	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	$\Delta I_{CC}$	$V_{CC}-2.1$	4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
An, Bn	0.83
OE	0.64
DIR	0.15

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC245 CD54/74ACT245

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3* 5†	— 2.8 1.8	108 12 8.6	— 2.1 1.7	120 13.4 9.6	ns
Output Disable to Output	t <sub>PLZ</sub> t <sub>PHZ</sub>	1.5 3.3 5	— 3.9 2.5	150 15 12	— 3.8 2.4	167 16.8 13.4	ns
Output Enable to Output	t <sub>PZL</sub> t <sub>PZH</sub>	1.5 3.3 5	— 3.9 2.5	150 18 12	— 3.8 2.4	167 20.1 13.4	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	66 Typ.		66 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output	t <sub>PLH</sub> t <sub>PHL</sub>	5†	1.9	9.6	1.8	10.6	ns
Output Disable to Output	t <sub>PLZ</sub> t <sub>PHZ</sub>	5	2.6	13	2.5	14.4	ns
Output Enable to Output	t <sub>PZH</sub> t <sub>PZL</sub>	5	2.6	13	2.5	14.4	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	79 Typ.		79 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>i</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

$\S C_{PD}$  is used to determine the dynamic power consumption, per channel.

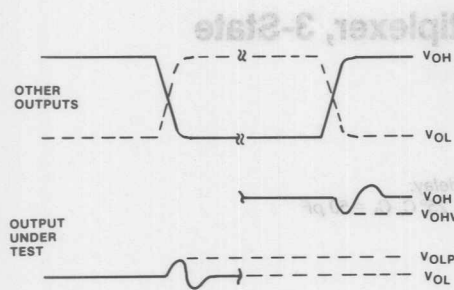
For AC series:  $PD = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT series:  $PD = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

# CD54/74AC245

## CD54/74ACT245

### PARAMETER MEASUREMENT INFORMATION

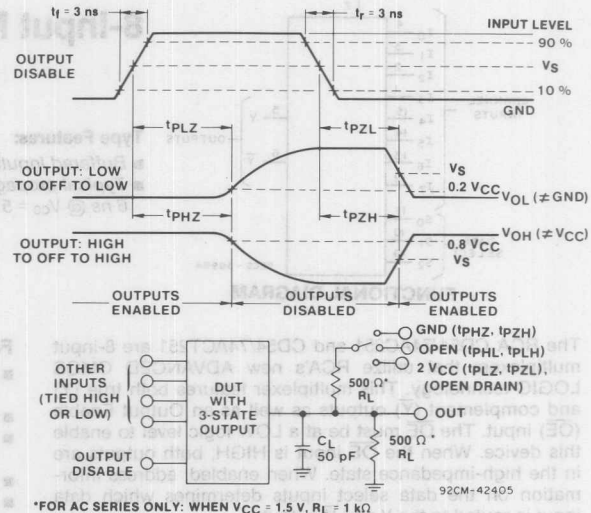


#### NOTES:

1.  $V_{OHV}$  and  $V_{OLP}$  ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:  
 $PRR \leq 1 \text{ MHz}$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ , SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.  
 IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1  $\mu\text{F}$  CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.



\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

Fig. 2 - Three-state propagation delay times and test circuit.

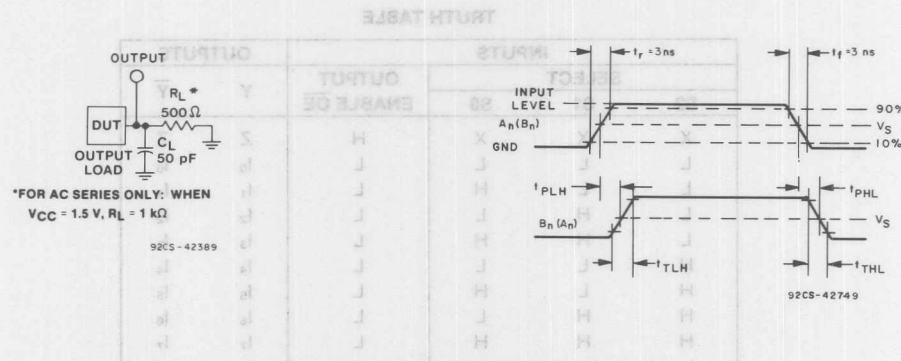
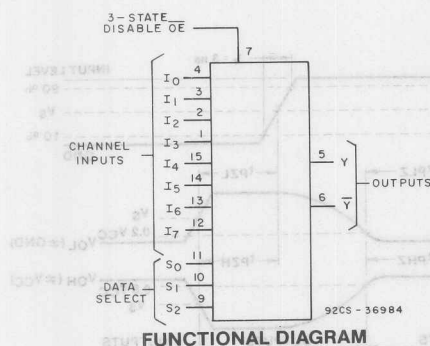


Fig. 3 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$





## 8-Input Multiplexer, 3-State

### Type Features:

- Buffered inputs
- Typical propagation delay:  
6 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

The RCA CD54/74AC251 and CD54/74ACT251 are 8-input multiplexers that utilize RCA's new ADVANCED CMOS LOGIC technology. This multiplexer features both true (Y) and complement ( $\bar{Y}$ ) outputs as well as an Output Enable ( $\bar{OE}$ ) input. The  $\bar{OE}$  must be at a LOW logic level to enable this device. When the  $\bar{OE}$  input is HIGH, both outputs are in the high-impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and  $\bar{Y}$  outputs.

The CD54AC251 and CD54ACT251 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC251 and CD74ACT251 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS			OUTPUTS	
SELECT			OUTPUT ENABLE $\bar{OE}$	Y $\bar{Y}$
S2	S1	S0		
X	X	X	H	Z    Z
L	L	L	L	$I_0$ $I_0$
L	L	H	L	$I_1$ $I_1$
L	H	L	L	$I_2$ $I_2$
L	H	H	L	$I_3$ $I_3$
H	L	L	L	$I_4$ $I_4$
H	L	H	L	$I_5$ $I_5$
H	H	L	L	$I_6$ $I_6$
H	H	H	L	$I_7$ $I_7$

H = High logic level

L = Low logic level

X = Irrelevant

Z = High impedance (off)

$I_0, I_1, \dots, I_7$  = The level of the respective input

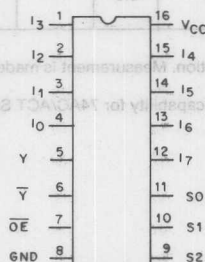
CD54/74ACT251	CD54/74AC251	CD54/74ACT251
5 V	5 V	5 V
5 V	5 V	5 V
5 V	5 V	5 V

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	.....	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	.....	±20 mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	.....	±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	.....	±50 mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	.....	±100 mA*
<b>POWER DISSIPATION PER PACKAGE (<math>P_O</math>):</b>		
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	.....	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	.....	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	.....	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	.....	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	.....	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	.....	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
<b>OPERATING-TEMPERATURE RANGE (<math>T_A</math>):</b>		
PACKAGE TYPE F	.....	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	.....	-40 to $+125^\circ\text{C}$
<b>STORAGE TEMPERATURE (<math>T_{stg}</math>)</b>	.....	-65 to $+150^\circ\text{C}$
<b>LEAD TEMPERATURE (DURING SOLDERING):</b>		
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	.....	+265° C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only	.....	+300° C
*(For up to 4 outputs per device; add ± 25 mA for each additional output.)		

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CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}^{*}$ : (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_i, V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	+125	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

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92CS-36831

### TERMINAL ASSIGNMENT

# CD54/74AC251 CD54/74ACT251

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
						+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>		1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V		
Low-Level Input Voltage	V <sub>IL</sub>		1.5 3 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V		
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05 -0.05 -0.05 -4	1.5 3 4.5 3	1.4 2.9 4.4 2.58	— — — —	1.4 2.9 4.4 2.48	— — — —	1.4 2.9 4.4 2.4	— — — —	V	
		# *	-24 -75 -50	4.5 5.5 5.5	3.94 — —	— — —	3.8 3.85 —	— — —	3.7 — 3.85	— — —		
			V <sub>IH</sub> or V <sub>IL</sub>	0.05 0.05 0.05 12 24	1.5 3 4.5 3 4.5	— — — — —	0.1 0.1 0.1 0.36 0.36	— — — — —	0.1 0.1 0.1 0.44 0.44	— — — — —	0.1 0.1 0.1 0.5 0.5	V
				# *	75 50	5.5 5.5	— —	— —	— —	1.65 —	— —	1.65 1.65
	V <sub>CC</sub> or GND				5.5	—	±0.1	—	±1	—	±1	μA
	3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA
	Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# CD54/74AC251 CD54/74ACT251

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	V <sub>cc</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS		
			+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	V <sub>IH</sub>	4.5 to 5.5	2	—	2	—	2	—	V		
Low-Level Input Voltage	V <sub>IL</sub>	4.5 to 5.5	—	0.8	—	0.8	—	0.8	V		
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		#	-24	4.5	3.94	—	3.8	—	3.7	—	
		*	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		#	24	4.5	—	0.36	—	0.44	—	0.5	
		*	75	5.5	—	—	—	1.65	—	—	
		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>cc</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I <sub>oz</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>cc</sub> or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I <sub>cc</sub>	V <sub>cc</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>cc</sub>	V <sub>cc</sub> -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

### ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
S0, S1, S2	1
OE	1
I <sub>0</sub> - I <sub>7</sub>	1

\*Unit load is ΔI<sub>cc</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

**SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$** 

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Y Output	$t_{PLH}$ $t_{PHL}$	1.5 3.3* 5†	— 3.7 2.4	152 16.9 12.1	— 3.5 2.3	169 18.9 13.5	ns
Data to $\bar{Y}$ Output	$t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 4 2.7	166 18.6 13.3	— 3.8 2.5	186 20.9 14.9	ns
Select to Y Output	$t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 5.1 3.3	204 22.8 16.3	— 4.7 3.1	228 25.5 18.2	ns
Select to $\bar{Y}$ Output	$t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 5.4 3.6	219 24.5 17.5	— 5 3.4	245 27.4 19.6	ns
Output Enable and Output Disable to Output	$t_{PZH}$ $t_{PZL}$ $t_{PHZ}$ $t_{PLZ}$	1.5 3.3 5	— 3.7 2.4	152 18.2 12.1	— 3.5 2.3	169 20.3 13.5	ns
Power Dissipation Capacitance	$C_{PD}$ §	—	—	—	—	—	pF
Input Capacitance	$C_i$	—	—	10	—	10	pF
3-State Output Capacitance	$C_o$	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§ $C_{PD}$  is used to determine the dynamic power consumption, per device.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency

$C_L$  = output load capacitance

$V_{CC}$  = supply voltage.

**SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$** 

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Y Output	$t_{PLH}$ $t_{PHL}$	5†	2.4	12.1	2.3	13.5	ns
Data to $\bar{Y}$ Output	$t_{PLH}$ $t_{PHL}$	5	2.7	13.3	2.5	14.9	ns
Select to Y Output	$t_{PLH}$ $t_{PHL}$	5	3.3	16.3	3.1	18.2	ns
Select to $\bar{Y}$ Output	$t_{PLH}$ $t_{PHL}$	5	3.6	17.5	3.4	19.6	ns
Output Enable and Output Disable to Output	$t_{PZH}$ $t_{PZL}$ $t_{PHZ}$ $t_{PLZ}$	5	2.4	12.1	2.3	13.5	ns
Power Dissipation Capacitance	$C_{PD}$ §	—	—	—	—	—	pF
Input Capacitance	$C_i$	—	—	10	—	10	pF
3-State Output Capacitance	$C_o$	—	—	15	—	15	pF

† min. is @ 5.5 V  
max. is @ 4.5 V

min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

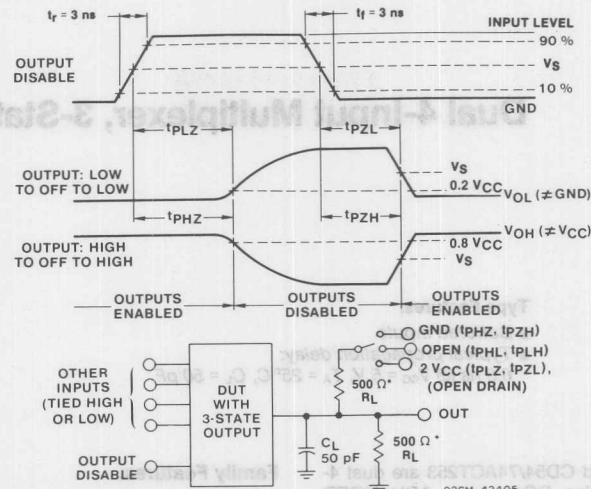
§ $C_{PD}$  is used to determine the dynamic power consumption, per device.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency

$C_L$  = output load capacitance

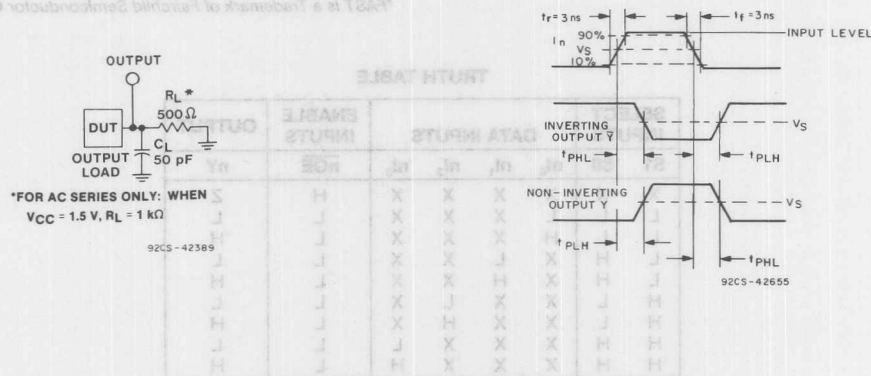
$V_{CC}$  = supply voltage.





\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

Fig. 1 - Three-state propagation delay times and test circuit.



\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

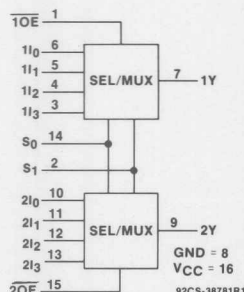
Fig. 2 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_s$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_s$	0.5 $V_{CC}$	0.5 $V_{CC}$

# CD54/74AC253

## CD54/74ACT253

Advance Information



FUNCTIONAL DIAGRAM

The RCA CD54/74AC253 and CD54/74ACT253 are dual 4-input multiplexers that utilize RCA's new ADVANCED CMOS LOGIC technology. One of the four sources for each section is selected by the common Select inputs, S0 and S1. When the Output Enable ( $\overline{1OE}$  or  $\overline{2OE}$ ) is HIGH, the output is in the high-impedance state.

The CD54AC253 and CD54ACT253 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC253 and CD74ACT253 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix).

## Dual 4-Input Multiplexer, 3-State

### Type Features:

- Buffered inputs
- Typical propagation delay:  
6.3 ns @  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50 pF$

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24$ -mA output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				ENABLE INPUTS	OUTPUT
S1	S0	nl <sub>0</sub>	nl <sub>1</sub>	nl <sub>2</sub>	nl <sub>3</sub>	$\overline{nOE}$	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs S1 and S0 are common to both sections.

H = High level

L = Low level

X = Don't care

Z = High impedance

CD54/74AC253	CD54/74ACT253	Input Level
3V	3V	Input Level
2.5V	2.5V	Input Switching Voltage $V_i$
2.5V	2.5V	Output Switching Voltage $V_o$

File Number 1985

# CD54/74AC253 CD54/74ACT253

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	$-55$ to $+125^\circ\text{C}$
PACKAGE TYPE E, M	$-40$ to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	$-65$ to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

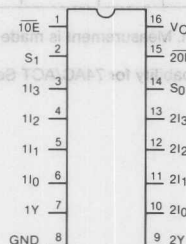
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	$-40$	$+125$	$^\circ\text{C}$
CD54 Types	$-55$	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.



92CS-36832R1

## TERMINAL ASSIGNMENT

# STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS		AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)	V <sub>CC</sub> (V)	MIN.	MAX.	MIN.	MAX.	MIN.	
High-Level Input Voltage	V <sub>IH</sub>		1.5	1.2	—	1.2	—	1.2	—	V	
			3	2.1	—	2.1	—	2.1	—		
			5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage	V <sub>IL</sub>		1.5	—	0.3	—	0.3	—	0.3	V	
			3	—	0.9	—	0.9	—	0.9		
			5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	3.85	—	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	1.65	—	—	—	
			50	5.5	—	—	—	—	1.65	—	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	$V_{CC}$ (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS		
			+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	V <sub>IH</sub>		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V <sub>IL</sub>		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> #	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> #	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	1.65	—	—	—	
			50	5.5	—	—	—	—	1.65	—	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	5.5	—	8	—	80	—	160	μA	
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
S0, S1, nI <sub>0</sub> , nI <sub>1</sub> nOE	1 0.83

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.



# CD54/74AC253

# CD54/74ACT253

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: S0, S1, to Y	$t_{PLH}$ $t_{PHL}$	1.5 3.3* 5†	— 5.4 3.6	224 25.1 17.9	— 5.2 3.4	250 28 20	ns
nI to Y	$t_{PLH}$ $t_{PHL}$	1.5 3.3 5	— 3.6 2.4	149 16.7 11.9	— 3.4 2.3	166 18.6 13.3	ns
Output Enable, Output Disable to Y	$t_{PLZ}$ $t_{PHZ}$ $t_{PZL}$ $t_{PZH}$	— 1.5 3.3 5	— 3.1 2.1	129 15.5 10.3	— 2.9 1.9	144 17.3 11.5	ns
Power Dissipation Capacitance	$C_{PD}$ §	—	—	—	—	—	pF
Input Capacitance	$C_i$	—	—	10	—	10	pF
3-State Output Capacitance	$C_o$	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§ $C_{PD}$  is used to determine the dynamic power consumption, per multiplexer.  
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

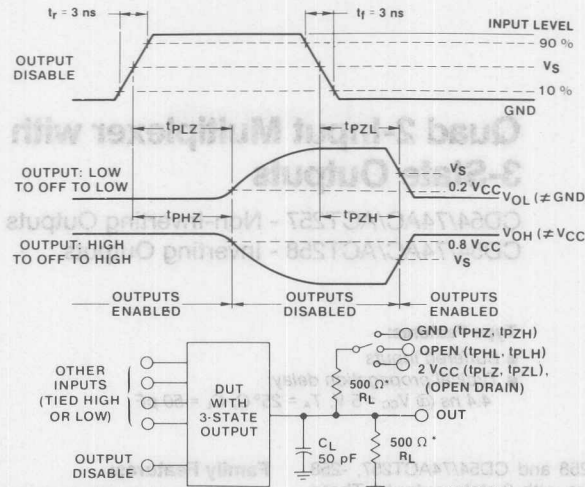
CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: S0, S1, to Y	$t_{PLH}$ $t_{PHL}$	5†	3.9	19.3	3.8	22	ns
nI to Y	$t_{PLH}$ $t_{PHL}$	5	3.3	16.2	3.1	18	ns
Output Enable, Output Disable to Y	$t_{PLZ}$ $t_{PHZ}$ $t_{PZL}$ $t_{PZH}$	5	2.3	11.3	2.1	12.6	ns
Power Dissipation Capacitance	$C_{PD}$ §	—	—	—	—	—	pF
Input Capacitance	$C_i$	—	—	10	—	10	pF
3-State Output Capacitance	$C_o$	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

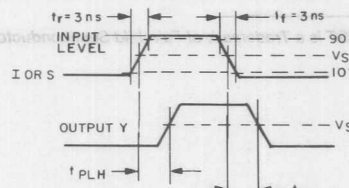
§ $C_{PD}$  is used to determine the dynamic power consumption, per multiplexer.  
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

# CD54/74AC253 CD54/74ACT253



92CM-42405

Fig. 1 - Three-state propagation delay waveforms and test circuit.

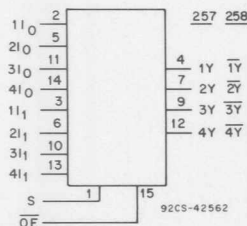


92CS-42611

Fig. 2 - Propagation delay times and test circuit.

Output Enable	Input Level	Data Input	Output
H	X	X	X
L	X	X	X
L	L	X	X
L	H	X	X
L	L	L	L
L	H	L	L

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$



FUNCTIONAL DIAGRAM

## Quad 2-Input Multiplexer with 3-State Outputs

CD54/74AC/ACT257 - Non-Inverting Outputs  
CD54/74AC/ACT258 - Inverting Outputs

### Type Features:

- Buffered inputs
- Typical propagation delay:  
4.4 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

The RCA CD54/74AC257, -258 and CD54/74ACT257, -258 are quad 2-input multiplexers with 3-state outputs. These devices utilize RCA's new ADVANCED CMOS LOGIC technology. Each of these devices selects four bits of data from two sources under the control of a common Select input (S). The Output Enable ( $\overline{OE}$ ) is active LOW. When  $\overline{OE}$  is HIGH, all of the outputs (Y or  $\overline{Y}$ ) are in the high-impedance state regardless of all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the CD54/74AC/ACT257 and CD54/74AC/ACT258. The state of the Select input determines the particular register from which the data comes. The CD54/74AC/ACT257 and CD54/74AC/ACT258 can also be used as function generators.

The CD54AC/ACT257 and CD54AC/ACT258 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT257 and CD74AC/ACT258 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix).

FUNCTION TABLE

Output Enable	Select Input	Data Inputs		257 Outputs	258 Outputs
$\overline{OE}$	S	$I_0$	$I_1$	Y	$\overline{Y}$
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High level voltage

L = Low level voltage

Z = High impedance (off) state.

X = Don't care

Input Level	5.0 V	5.0 V
Input Switching Voltage, $V_i$	5.0 V	5.0 V
Output Switching Voltage, $V_o$	5.0 V	5.0 V

# **MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	
	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\* (For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

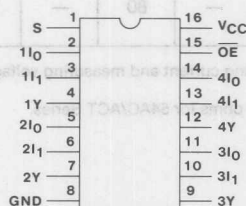
## **RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range)			
	AC Types	1.5	5.5
	ACT Types	4.5	5.5
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
	CD74 Types	-40	$+125^\circ\text{C}$
	CD54 Types	-55	$+125^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)			
	0	50	ns/V
	0	20	ns/V
	0	10	ns/V

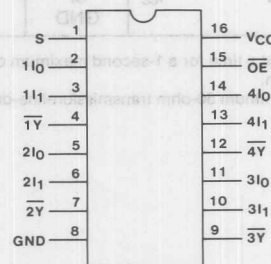
\* Unless otherwise specified, all voltages are referenced to ground.

## **TERMINAL ASSIGNMENT DIAGRAMS**



92CS-38420RI

CD54/74AC/ACT257



92CS-39815

CD54/74AC/ACT258

# CD54/74AC257, CD54/74AC258 CD54/74ACT257, CD54/74ACT258

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
						+25		0 to +70		-40 to +125(74)		
								-40 to +85		-55 to +125(54)		
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V <sub>IH</sub>					1.5	1.2	—	1.2	—	1.2	—	V
					3	2.1	—	2.1	—	2.1	—	
					5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V <sub>IL</sub>					1.5	—	0.3	—	0.3	—	0.3	V
					3	—	0.9	—	0.9	—	0.9	
					5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V <sub>OH</sub>			V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
				-0.05	3	2.9	—	2.9	—	2.9	—	
				-0.05	4.5	4.4	—	4.4	—	4.4	—	
				-4	3	2.58	—	2.48	—	2.4	—	
				-24	4.5	3.94	—	3.8	—	3.7	—	
				-75	5.5	—	—	3.85	—	—	—	
				-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V <sub>OL</sub>			V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
				0.05	3	—	0.1	—	0.1	—	0.1	
				0.05	4.5	—	0.1	—	0.1	—	0.1	
				12	3	—	0.36	—	0.44	—	0.5	
				24	4.5	—	0.36	—	0.44	—	0.5	
				75	5.5	—	—	—	1.65	—	—	
				50	5.5	—	—	—	—	—	1.65	
Input Leakage Current			V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current			V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI			V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.



# CD54/74AC257, CD54/74AC258

## CD54/74ACT257, CD54/74ACT258

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS		
			+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	$V_{IH}$	4.5 to 5.5	2	—	2	—	2	—	V		
Low-Level Input Voltage	$V_{IL}$	4.5 to 5.5	—	0.8	—	0.8	—	0.8	V		
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	4.5	4.4	—	4.4	—	4.4	V	
		#	-24	4.5	3.94	—	3.8	—	3.7		
		*	-75	5.5	—	—	3.85	—	—		
		*	-50	5.5	—	—	—	—	3.85		
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.05	4.5	—	0.1	—	0.1	—	V	
		#	24	4.5	—	0.36	—	0.44	—		0.5
		*	75	5.5	—	—	1.65	—	—		
		*	50	5.5	—	—	—	—	1.65		
Input Leakage Current	$I_i$	$V_{CC}$ or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	$I_{OZ}$	$V_{IH}$ or $V_{IL}$	—	—	—	—	—	—	—	—	
		$V_O = V_{CC}$ or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	$I_{CC}$	$V_{CC}$ or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	$\Delta I_{CC}$	$V_{CC}-2.1$	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

## ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
Data	0.83
S	1.27
OE	1.27

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

**SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$** 

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: I <sub>n</sub> to Y	257	t <sub>PLH</sub> t <sub>PHL</sub> 1.5 3.3* 5†	— 2.5 1.7	105 11.8 8.4	— 2.4 1.6	117 13 9.3	ns
S to Y	257	t <sub>PLH</sub> t <sub>PHL</sub> 1.5 3.3 5	— 3.6 2.4	150 16.8 12	— 3.5 2.3	168 18.8 13.4	ns
OE to Y	257	t <sub>PLZ</sub> t <sub>PHZ</sub> t <sub>PZL</sub> t <sub>PZH</sub> 1.5 3.3 5	— 4 2.7	165 19.8 13.2	— 3.8 2.5	184 22.1 14.7	ns
I <sub>n</sub> to Y	258	t <sub>PLH</sub> t <sub>PHL</sub> 1.5 3.3 5	— 2.2 1.4	90 10.1 7.2	— 2 1.3	100 11.2 8	ns
S to Y	258	t <sub>PLH</sub> t <sub>PHL</sub> 1.5 3.3 5	— 3.6 2.4	150 16.8 12	— 3.5 2.3	168 18.8 13.4	ns
OE to Y	258	t <sub>PLZ</sub> t <sub>PHZ</sub> t <sub>PZL</sub> t <sub>PZH</sub> 1.5 3.3 5	— 4 2.7	165 19.8 13.2	— 3.8 2.5	184 22.1 14.7	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	130 Typ.		130 Typ.		pF
Input Capacitance	C <sub>i</sub>	—	10		10		pF
3-State Output Capacitance	C <sub>o</sub>	—	15		15		pF

**SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$** 

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: $I_n$ to Y	257	$t_{PLH}$ $t_{PHL}$	5†	1.9 9.6	1.8	10.7	ns
S to Y	257	$t_{PLH}$ $t_{PHL}$	5	2.8 13.9	2.6	15.4	ns
$\overline{OE}$ to Y	257	$t_{PLZ}$ $t_{PHZ}$ $t_{PZL}$ $t_{PZH}$	5	3 14.5	2.8	16.1	ns
$I_n$ to $\overline{Y}$	258	$t_{PLH}$ $t_{PHL}$	5	1.7 8.4	1.6	9.3	ns
S to $\overline{Y}$	258	$t_{PLH}$ $t_{PHL}$	5	2.8 13.9	2.6	15.4	ns
$\overline{OE}$ to $\overline{Y}$	258	$t_{PLZ}$ $t_{PHZ}$ $t_{PZL}$ $t_{PZH}$	5	3 14.5	2.8	16.1	ns
Power Dissipation Capacitance	$C_{PD}\S$	—	170 Typ.		170 Typ.		pF
Input Capacitance	$C_i$	—	10		10		pF
3-State Output Capacitance	$C_o$	—	15		15		pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§ $C_{PD}$  is used to determine the dynamic power consumption per multiplexer.

For AC Series:  $P_D = C_{PD} V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o)$

For ACT Series:  $P_D = C_{PD} V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$

where  $f_i$  = input frequency

$f_o$  = output frequency

$C_L$  = output load capacitance

$V_{CC}$  = supply voltage.

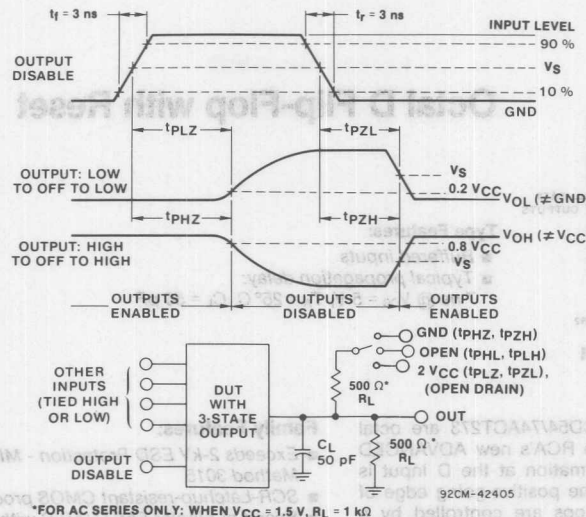


Fig. 1 - Three-state propagation delay waveforms and test circuit.

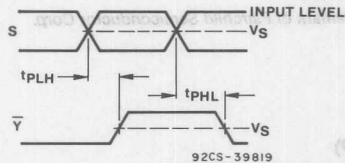


Fig. 2 - Select to output propagation delays (AC/ACT257).

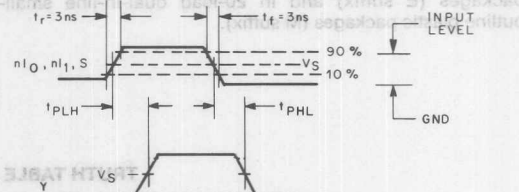
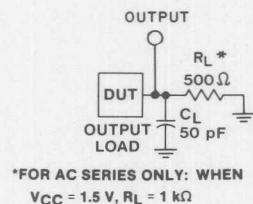


Fig. 3 - Inputs or select to output propagation delays (AC/ACT258).



\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

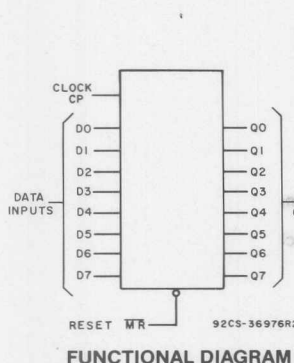
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Fig. 4 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$

# CD54/74AC273 CD54/74ACT273

Product Preview



## Octal D Flip-Flop with Reset

### Type Features:

- Buffered inputs
- Typical propagation delay:  
7 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

The RCA CD54/74AC273 and CD54/74ACT273 are octal D flip-flops with reset that utilize RCA's new ADVANCED CMOS LOGIC technology. Information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. All eight flip-flops are controlled by a common clock (CP) and a common reset ( $\overline{\text{MR}}$ ). Resetting is accomplished by a low-voltage level independent of the clock.

The CD54AC273 and CD54ACT273 are supplied in 20-lead dual-in-line ceramic packages (F suffix). The CD74AC273 and CD74ACT273 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUTS
RESET ( $\overline{\text{MR}}$ )	CLOCK CP	DATA $D_n$	$Q_n$
L	X	X	L
H		H	H
H		L	L
H	L	X	$Q_0$

H = High level (steady state)

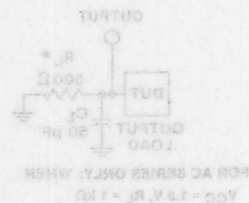
L = Low level (steady state)

X = Irrelevant

= Transition from Low to High level

$Q_0$  = The level of Q before the indicated steady-state input conditions were established

Input Level	Input Switching Voltage, $V_i$	Output Switching Voltage, $V_o$
3 V	0.5 $V_{CC}$	0.5 $V_{CC}$
1.5 V	0.5 $V_{CC}$	0.5 $V_{CC}$
0.5 V	0.5 $V_{CC}$	0.5 $V_{CC}$



# CD54/74AC273 CD54/74ACT273

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

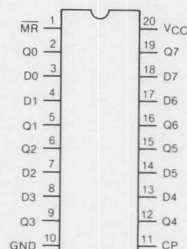
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.



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## TERMINAL ASSIGNMENT

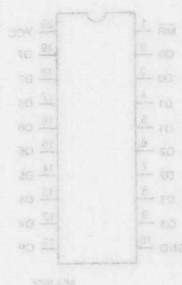


# STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
						+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
			V <sub>i</sub> (V)	I <sub>o</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>		1.5 3.0 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V		
Low-Level Input Voltage	V <sub>IL</sub>		1.5 3.0 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V		
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	1.5	1.40	—	1.40	—	1.40	—	V	
			-0.05	3.0	2.90	—	2.90	—	2.90	—		
			-0.05	4.5	4.40	—	4.40	—	4.40	—		
			-4	3.0	2.58	—	2.48	—	2.40	—		
		# *	-24	4.5	3.94	—	3.80	—	3.70	—		
			-75	5.5	—	—	3.85	—	—	—		
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	1.5	—	0.1	—	0.1	—	0.1	V	
			0.05	3.0	—	0.1	—	0.1	—	0.1		
			0.05	4.5	—	0.1	—	0.1	—	0.1		
		# *	12	3.0	—	0.36	—	0.44	—	0.5		
			24	4.5	—	0.36	—	0.44	—	0.5		
			75	5.5	—	—	—	1.65	—	—		
Input Leakage Current	I <sub>i</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA		
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.



TERMINAL ASSIGNMENT

# STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS		
			+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	V <sub>IH</sub>		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V <sub>IL</sub>		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.80	—	3.70	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	4.5	—	0.1	—	0.1	—	0.10	V
			24	4.5	—	0.36	—	0.44	—	0.50	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	5.5	—	8	—	80	—	160	μA	
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
Dn	0.5
MR	0.57
CP	1

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC273 CD54/74ACT273

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t <sub>SU</sub>	1.5 3.3* 5†	—	—	—	—	ns
Hold Time	t <sub>H</sub>	1.5 3.3 5	—	—	—	—	ns
Removal Time MR to CP	t <sub>REM</sub>	1.5 3.3 5	—	—	—	—	ns
MR Pulse Width	t <sub>W</sub>	1.5 3.3 5	—	—	—	—	ns
CP Pulse Width	t <sub>W</sub>	1.5 3.3 5	—	—	—	—	ns
CP Frequency	f <sub>MAX</sub>	1.5 3.3 5	—	—	—	—	MHz

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

5 V: min is @ 4.75 V for 0 to +70°C

SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3* 5†	— 4 2.7	166 18.6 13.3	— 3.8 2.5	186 20.9 14.9	ns
MR to Qn	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 3.7 2.5	152 16.9 12.1	— 3.5 2.3	169 18.9 13.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	—	10	—	10	pF
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per flip-flop.

$$P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) \text{ where } f_i = \text{input frequency}$$

$$f_o = \text{output frequency}$$

$$C_L = \text{output load capacitance}$$

$$V_{CC} = \text{supply voltage.}$$

# CD54/74AC273

## CD54/74ACT273

### PREREQUISITE FOR SWITCHING — ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t <sub>SU</sub>	5*		—		—	ns
Hold Time	t <sub>H</sub>	5		—		—	ns
Removal Time MR to CP	t <sub>REM</sub>	5		—		—	ns
MR Pulse Width	t <sub>W</sub>	5		—		—	ns
CP Pulse Width	t <sub>W</sub>	5		—		—	ns
CP Frequency	f <sub>max</sub>	5		—		—	MHz

SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn	t <sub>PLH</sub>	5*	2.7	13.3	2.5	14.9	ns
	t <sub>PHL</sub>						
MR to Qn	t <sub>PLH</sub>	5	2.7	13.3	2.5	14.9	ns
	t <sub>PHL</sub>						
Power Dissipation Capacitance	C <sub>PD</sub> †	—					pF
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF

\*min. is @ 5.5 V  
max. is @ 4.5 V

min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

†C<sub>PD</sub> is used to determine the dynamic power consumption, per flip-flop.

P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>i</sub> + Σ(C<sub>L</sub> V<sub>CC</sub><sup>2</sup> f<sub>o</sub>) + V<sub>CC</sub> ΔI<sub>CC</sub> where f<sub>i</sub> = input frequency  
f<sub>o</sub> = output frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.

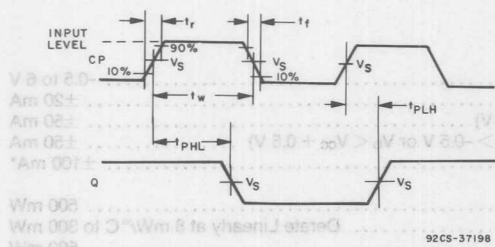


Fig. 1 - Propagation delay times and clock pulse width.

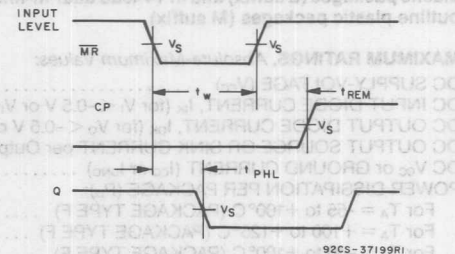


Fig. 2 - Prerequisite and propagation delay times for master reset

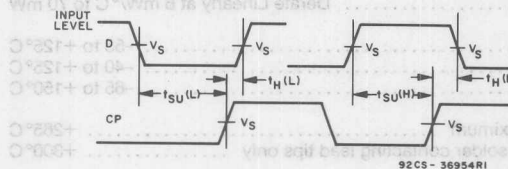


Fig. 3 - Prerequisite for clock.

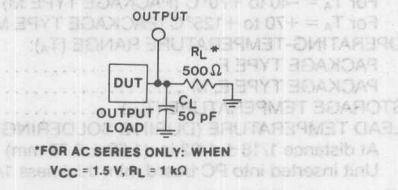
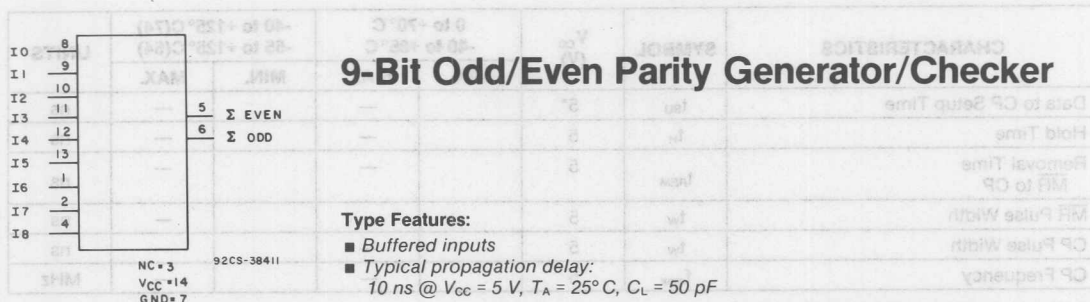


Fig. 4 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V <sub>CC</sub>	3 V
Input Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	1.5 V
Output Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>



### FUNCTIONAL DIAGRAM

The RCA-CD54/74AC280 and CD54/74ACT280 are 9-bit odd/even parity generator/checkers that utilize RCA's new ADVANCED CMOS LOGIC technology. Both even and odd parity outputs are available for checking or generating parity for words up to nine bits long. Even parity is indicated ( $\Sigma E$  output is HIGH) when an even number of data inputs is HIGH. Odd parity is indicated ( $\Sigma O$  output is HIGH) when an odd number of data inputs is HIGH. Parity checking for words larger than nine bits can be accomplished by tying the  $\Sigma E$  output to any input of an additional AC/ACT280 parity checker.

The CD54AC280 and CD54ACT280 are supplied in 14-lead dual-in-line ceramic packages (F suffix). The CD74AC280 and CD74ACT280 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ )	$\pm 20\text{ mA}$
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ )	$\pm 50\text{ mA}$
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5\text{ V}$ or $V_O < V_{CC} + 0.5\text{ V}$ )	$\pm 50\text{ mA}$
DC $V_{CC}$ OR GROUND CURRENT ( $I_{CC}$ OR $I_{GND}$ )	$\pm 100\text{ mA}^*$
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79\text{ mm}$ ) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59\text{ mm}$ ) with solder contacting lead tips only	$+300^\circ\text{C}$

\* (For up to 4 outputs per device; add  $\pm 25\text{ mA}$  for each additional output.)

Fig. 8 - Propagation Delay

Input Level	Input Switching Voltage, $V_i$	Output Switching Voltage, $V_o$
3 V	0.5 V	0.5 V
1.5 V	0.5 V	0.5 V
0.5 V	0.5 V	0.5 V

File Number 1957



# RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40 -55	+125 +125	°C °C
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70		-40 to +125(74)		
							-40 to +85		-55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub>	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
		or V <sub>IL</sub>	-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
		#	-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub>	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
		or V <sub>IL</sub>	0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
		#	24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# CD54/74AC280 CD54/74ACT280

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS			TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
						+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> #	-0.05	4.5	4.4	—	4.4	—	4.4	—	V	
			-24	4.5	3.94	—	3.8	—	3.7	—		
			-75	5.5	—	—	3.85	—	—	—		
			-50	5.5	—	—	—	—	3.85	—		
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> #	0.05	4.5	—	0.1	—	0.1	—	0.1	V	
			24	4.5	—	0.36	—	0.44	—	0.5		
			75	5.5	—	—	—	1.65	—	—		
			50	5.5	—	—	—	—	1.65	—		
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA	
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

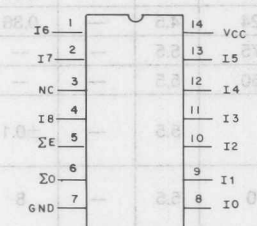
#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
All	1.43

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.



TERMINAL ASSIGNMENT

# CD54/74AC280 CD54/74ACT280

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Any Input to $\Sigma O$	$t_{PLH}$	1.5	—	243	—	270	ns
	$t_{PHL}$	3.3*	5.9	27.2	5.6	30.2	
Any Input to $\Sigma E$	$t_{PLH}$	1.5	—	243	—	270	ns
	$t_{PHL}$	3.3	5.9	27.2	5.6	30.2	
Power Dissipation Capacitance	$C_{PD}\S$	—	155 Typ.		155 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Any Input to $\Sigma O$	$t_{PLH}$	5†	3.9	19.4	3.7	21.6	ns
	$t_{PHL}$	5	3.9	19.4	3.7	21.6	
Power Dissipation Capacitance	$C_{PD}\S$	—	165 Typ.		165 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

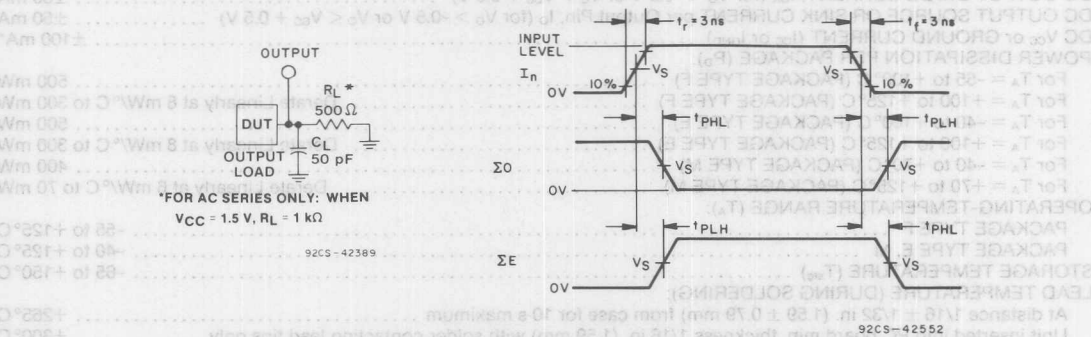
$\S C_{PD}$  is used to determine the dynamic power consumption, per package.

For AC series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency

$C_L$  = output load capacitance

$V_{CC}$  = supply voltage.

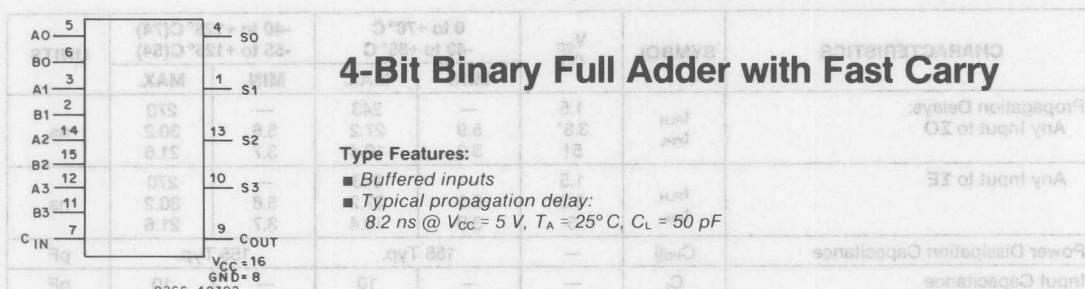


	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_s$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_s$	0.5 $V_{CC}$	0.5 $V_{CC}$

Fig. 1 - Propagation delay times and test circuit.

# CD54/74AC283

## CD54/74ACT283



The GE/RCA CD54/74AC283 and CD54/74ACT283 are 4-bit binary adders with fast carry which utilize GE/RCA's new ADVANCED CMOS LOGIC technology. These devices add two 4-bit binary numbers and generate a carry-out bit if the sum exceeds 15.

Because of the symmetry of the add function, this device can be used with either all active-HIGH operands (positive logic) or with all active-LOW operands (negative logic). When using positive logic, the carry-in input must be tied LOW if there is no carry-in.

The CD54AC/ACT283 are supplied in 16-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT283 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ )	$\pm 20\text{ mA}$
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ )	$\pm 50\text{ mA}$
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5\text{ V}$ or $V_O < V_{CC} + 0.5\text{ V}$ )	$\pm 50\text{ mA}$
DC $V_{CC}$ OR GROUND CURRENT ( $I_{CC}$ OR $I_{GND}$ )	$\pm 100\text{ mA}^*$

### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW

### OPERATING-TEMPERATURE RANGE ( $T_A$ ):

PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$

### STORAGE TEMPERATURE ( $T_{STG}$ )

	-65 to $+150^\circ\text{C}$
--	-----------------------------

### LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 $\pm$ 1/32 in. (1.59 $\pm$ 0.79 mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\* (For up to 4 outputs per device; add  $\pm 25\text{ mA}$  for each additional output.)

Input Level	Input Switching Voltage, $V_{IS}$	Output Switching Voltage, $V_{OS}$
$V_{CC}$	0.5 $V_{CC}$	0.5 $V_{CC}$
3 V	1.5 V	0.5 $V_{CC}$

Fig. 1 - Propagation delay times and test circuit

# CD54/74AC283

## CD54/74ACT283

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}^*$ : (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	+125	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

**STATIC ELECTRICAL CHARACTERISTICS: AC Series**

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.



# CD54/74AC283 CD54/74ACT283

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS			TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
						+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V	
			-24	4.5	3.94	—	3.8	—	3.7	—		
			-75	5.5	—	—	3.85	—	—	—		
			-50	5.5	—	—	—	—	3.85	—		
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	4.5	—	0.1	—	0.1	—	0.1	V	
			24	4.5	—	0.36	—	0.44	—	0.5		
			75	5.5	—	—	—	1.65	—	—		
			50	5.5	—	—	—	—	—	1.65		
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA	
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5		2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
A1, B1, A3, B3	1.33
A2, B2	1.5
A4, B4	1.0
$C_{IN}$	0.83

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC283

## CD54/74ACT283

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ 

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: $A_n$ or $B_n$ to $C_{out}$ $C_{in}$ to $S_n$ $C_{in}$ to $C_{out}$	$t_{PLH}$	1.5	—	196	—	219	ns
	$t_{PHL}$	3.3*	5.1	22	4.9	24.6	
		5†	3.3	15.7	3.1	17.6	
$A_n$ or $B_n$ to $S_n$	$t_{PLH}$	1.5	—	204	—	228	ns
	$t_{PHL}$	3.3	5.3	22.8	5.1	25.5	
		5	3.4	16.3	3.3	18.2	
Power Dissipation Capacitance	$C_{PD}\S$	—	120 Typ.		120 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ 

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: $A_n$ or $B_n$ to $C_{out}$ $C_{in}$ to $S_n$ $C_{in}$ to $C_{out}$	$t_{PLH}$	5‡	3.3	15.7	3.1	17.6	ns
	$t_{PHL}$						
$A_n$ or $B_n$ to $S_n$	$t_{PLH}$	5‡	3.4	16.3	3.3	18.2	ns
	$t_{PHL}$						
Power Dissipation Capacitance	$C_{PD}\S$	—	120 Typ.		120 Typ.		pF
Input Capacitance	$C_i$	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

‡5 V: min. is @ 5.5 V  
max. is @ 4.5 V

§5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

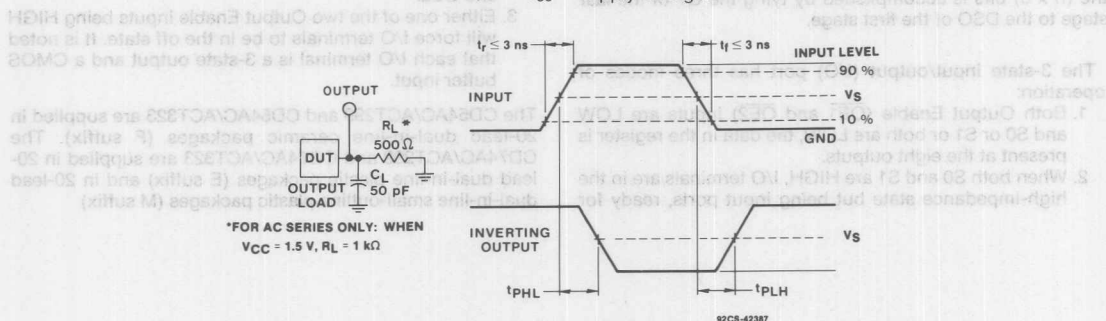
§ $C_{PD}$  is used to determine the dynamic power consumption, per function.

For AC Series:  $PD = V_{CC}^2 f_i (C_{PD} + C_L)$

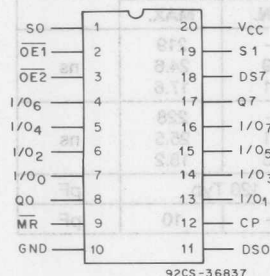
For ACT Series:  $PD = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency

$C_L$  = output load capacitance

$V_{CC}$  = supply voltage.



	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$



## 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

CD54/74AC/ACT299 - Asynchronous Reset

CD54/74AC/ACT323 - Synchronous Reset

### Type Features:

- Buffered inputs
- Typical propagation delay:  
6 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

### TERMINAL ASSIGNMENT

The RCA CD54/74AC299, -323 and CD54/74ACT299, -323 are 3-state, 8-input universal shift/storage registers with common parallel I/O pins. These devices utilize RCA's new ADVANCED CMOS LOGIC technology. These registers have four synchronous-operating modes controlled by the two select inputs as shown in the Mode Select (S0, S1) table. The Mode Select, the Serial Data (DSO, DS7), and the Parallel Data (I/O<sub>0</sub> - I/O<sub>7</sub>) respond only to the LOW-TO-HIGH transition of the clock (CP) pulse. S0, S1 and Data inputs must be present one setup time prior to the positive transition of the clock.

With the CD54/74AC/ACT299, the Master Reset ( $\overline{\text{MR}}$ ) is an asynchronous active-LOW input. When  $\overline{\text{MR}}$  is LOW, the register is cleared regardless of the status of all other inputs. With the CD54/74AC/ACT323, the Master Reset ( $\overline{\text{MR}}$ ) clears the register in sync with the clock input. The register can be expanded by cascading same units by tying the serial output (Q0) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DSO) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DSO of the first stage.

The 3-state input/output (I/O) port has three modes of operation:

1. Both Output Enable ( $\overline{\text{OE1}}$  and  $\overline{\text{OE2}}$ ) inputs are LOW and S0 or S1 or both are LOW, the data in the register is present at the eight outputs.
2. When both S0 and S1 are HIGH, I/O terminals are in the high-impedance state but being input ports, ready for

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

parallel data to be loaded into eight registers with one clock transition regardless of the status of  $\overline{\text{OE1}}$  and  $\overline{\text{OE2}}$ .

3. Either one of the two Output Enable inputs being HIGH will force I/O terminals to be in the off state. It is noted that each I/O terminal is a 3-state output and a CMOS buffer input.








The CD54AC/ACT299 and CD54AC/ACT323 are supplied in 20-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT299 and CD74AC/ACT323 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix)

Output Switching Voltage, $V_o$	Input Switching Voltage, $V_i$	Input Level
0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>	3 V
0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>	1.8 V
0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>	3 V

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# CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

## MODE SELECT — FUNCTION TABLE REGISTER OPERATING MODES

FUNCTION	INPUTS							REGISTER OUTPUTS					
	$\overline{MR}$	CP	S0	S1	DS0	DS7	I/O <sub>n</sub>	Q0	Q1	...	Q6	Q7	
Reset (Clear)	L	X*	X	X	X	X	X	L	L	...	L	L	
Shift Right	H		h	l	l	X	X	L	Q <sub>0</sub>	...	Q <sub>5</sub>	Q <sub>6</sub>	
	H		h	l	h	X	X	H	Q <sub>0</sub>	...	Q <sub>5</sub>	Q <sub>6</sub>	
Shift Left	H		l	h	X	l	X	q <sub>1</sub>	q <sub>2</sub>	...	q <sub>7</sub>	L	
	H		l	h	X	h	X	q <sub>1</sub>	q <sub>2</sub>	...	q <sub>7</sub>	H	
Hold (do nothing)	H		l	l	X	X	X	Q <sub>0</sub>	q <sub>1</sub>	...	Q <sub>6</sub>	q <sub>7</sub>	
Parallel Load	H		h	h	X	X	l	L	L	...	L	L	
	H		h	h	X	X	h	H	H	...	H	H	

\*On CD54/74AC/ACT323, CP must be in transition from the LOW-to-HIGH state to Reset (Clear).

## MODE SELECT — FUNCTION TABLE 3-STATE I/O PORT OPERATING MODE

FUNCTION	INPUTS					INPUTS/OUTPUTS
	OE1	OE2	S0	S1	Qn (Register)	I/O <sub>0</sub> . . . I/O <sub>7</sub>
Read Register	L	L	L	X	L	L
	L	L	L	X	H	H
	L	L	X	L	L	L
	L	L	X	L	H	H
Load Register	X	X	H	H	Qn = I/O <sub>n</sub>	I/O <sub>n</sub> = Inputs
Disable I/O	H	X	X	X	X	(Z)
	X	H	X	X	X	(Z)

H = Input voltage high level.

h = Input voltage high one set-up time prior clock transition.

L = Input voltage low level.

l = Input voltage low one set-up time prior clock transition.

q<sub>n</sub> = Lower case letters indicate the state of the referenced output one set-up time prior clock transition.

X = Voltage level on logic status don't care.

Z = Output in high-impedance state.

= Low-to-high clock transition.

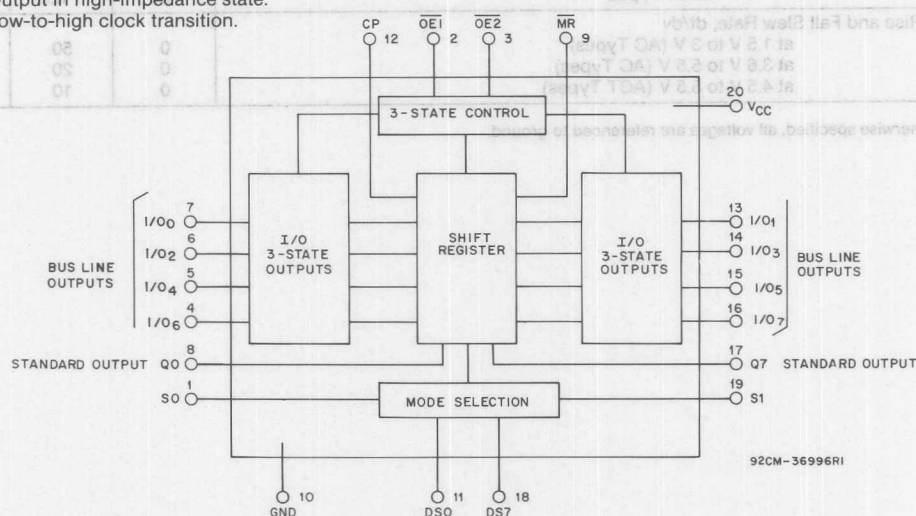


Fig. 1 - Functional diagram.

# CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	.....	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	.....	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	.....	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	.....	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	.....	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):		
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	.....	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	.....	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	.....	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	.....	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	.....	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	.....	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):		
PACKAGE TYPE F	.....	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	.....	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{STG}$ )	.....	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 $\pm$ 1/32 in. (1.59 $\pm$ 0.79 mm) from case for 10 s maximum	.....	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only	.....	$+300^\circ\text{C}$

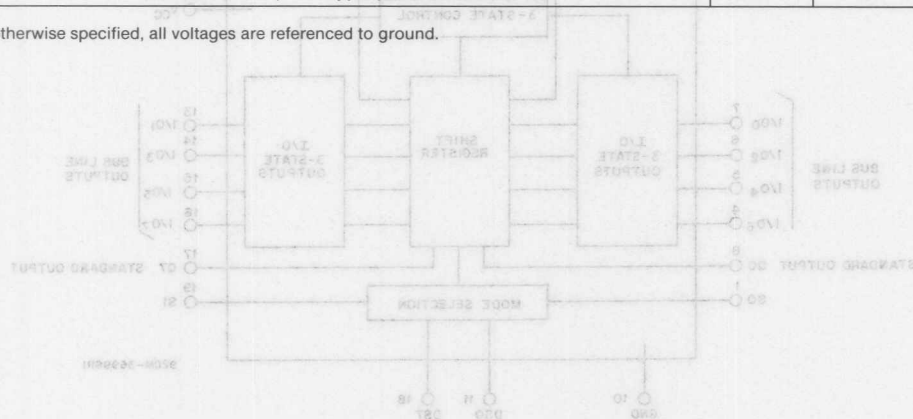
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.





# CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
				+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V <sub>IH</sub>		1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V	
Low-Level Input Voltage	V <sub>IL</sub>		1.5 3 5.5	— 0.3 —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
		# *	-24	4.5	3.94	—	3.8	—	3.7	—	V
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
			0.05	1.5	—	0.1	—	0.1	—	0.1	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	3	—	0.1	—	0.1	—	0.1	V
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
		# *	24	4.5	—	0.36	—	0.44	—	0.5	V
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-Stage Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	16
17	17
18	18
19	19
20	20
21	21
22	22
23	23
24	24
25	25
26	26
27	27
28	28
29	29
30	30
31	31
32	32
33	33
34	34
35	35
36	36
37	37
38	38
39	39
40	40
41	41
42	42
43	43
44	44
45	45
46	46
47	47
48	48
49	49
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61	61
62	62
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67	67
68	68
69	69
70	70
71	71
72	72
73	73
74	74
75	75
76	76
77	77
78	78
79	79
80	80
81	81
82	82
83	83
84	84
85	85
86	86
87	87
88	88
89	89
90	90
91	91
92	92
93	93
94	94
95	95
96	96
97	97
98	98
99	99
100	100

\*Unit load is defined as 1 unit specified in Table 1.  
Characteristics are at V<sub>CC</sub> = 5.5 V, T<sub>A</sub> = 25°C.

# CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
				+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V <sub>IH</sub>	—	4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V <sub>IL</sub>	—	4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		#	-24	4.5	3.94	—	3.8	—	3.7	—	
		*	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		#	24	4.5	—	0.36	—	0.44	—	0.5	
		*	75	5.5	—	—	1.65	—	—	—	
		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	—	5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>	—	—	—	—	—	—	—	—	μA
		V <sub>O</sub>	—	5.5	—	±0.5	—	±5	—	±10	
		V <sub>CC</sub> or GND	—	—	—	—	—	—	—	—	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*	
	299	323
S1, S2, $\overline{OE}1$ , $\overline{OE}2$	0.83	0.83
SL, CP	0.67	0.67
$\overline{MR}$	1.33	0.67

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

## PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Setup Time S1, S0, to CP	t <sub>SU</sub>	1.5 3.3* 5†	—	—	—	—	ns
Hold Time S1, S0 to CP	t <sub>H</sub>	1.5 3.3 5	—	—	—	—	ns
Setup Time (I/O)n, DS0, DS7 to CP	t <sub>SU</sub>	1.5 3.3 5	—	—	—	—	ns
Hold Time (I/O)n, DS0, DS7 to CP	t <sub>SU</sub>	1.5 3.3 5	—	—	—	—	ns
Maximum CP Frequency	f <sub>MAX</sub>	1.5 3.3 5	5.6 40 70	—	—	—	MHz
CP Pulse Width	t <sub>w</sub>	1.5 3.3 5	90 12.5 7	—	—	—	ns
MR Pulse Width	t <sub>w</sub>	1.5 3.3 5	—	—	—	—	ns
Recovery Time MR to CP 299	t <sub>REC</sub>	1.5 3.3 5	—	—	—	—	ns

\*3.3 V.min. is @ 3 V

†5 V.min. is @ 4.5 V

5 V.min. is @ 4.75 V for 0 to +70°C

SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q0, Q7	t <sub>PLH</sub>	1.5	—	144	—	162	ns
	t <sub>PHL</sub>	3.3* 5†	3.5 2.3	16.1 11.5	3.4 2.2	18.1 12.9	
CP to (I/O)n	t <sub>PLH</sub>	1.5	—	150	—	169	ns
	t <sub>PHL</sub>	3.3 5	3.6 2.4	16.8 12	3.5 2.3	18.9 13.5	
MR to Q0, Q7 (299 only)	t <sub>PLH</sub>	1.5	—	125	—	140	ns
	t <sub>PHL</sub>	3.3 5	3 2	14 10	2.9 1.9	15.7 11.2	
MR to (I/O)n	t <sub>PLH</sub>	1.5	—	155	—	174	ns
	t <sub>PHL</sub>	3.3 5	3.8 2.5	17.4 12.4	3.5 2.4	19.5 13.9	
Enable and Disable Times	t <sub>PZL</sub>	1.5	—	166	—	186	ns
	t <sub>PLZ</sub> t <sub>PHZ</sub>	3.3 5	4 2.7	20 13.3	3.8 2.6	22.4 14.9	
Power Dissipation Capacitance	C <sub>PD</sub> §	—	—	—	—	—	pF
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V.  
max. is @ 3 V.†5 V: min. is @ 5.5 V.  
max. is @ 4.5 V.5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C§C<sub>PD</sub> is used to determine the dynamic power consumption, per function.P<sub>D</sub> = C<sub>PD</sub>V<sub>CC</sub><sup>2</sup>f<sub>i</sub> + Σ (C<sub>L</sub>V<sub>CC</sub><sup>2</sup>f<sub>o</sub>) where f<sub>i</sub> = input frequencyf<sub>o</sub> = output frequencyC<sub>L</sub> = output load capacitanceV<sub>CC</sub> = supply voltage.

# CD54/74AC299, CD54/74AC323 CD54/74ACT299, CD54/74ACT323

## PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Setup Time S1, S0 to CP	t <sub>su</sub>	5*	—	—	—	—	ns
Hold Time S1, S0 to CP	t <sub>h</sub>	5	—	—	—	—	ns
Setup Time (I/O)n, DS0, DS7 to CP	t <sub>su</sub>	5	—	—	—	—	ns
Hold Time (I/O)n, DS0, DS7 to CP	t <sub>h</sub>	5	—	—	—	—	ns
Maximum CP Frequency	f <sub>max</sub>	5	70	—	—	—	MHz
CP Pulse Width	t <sub>w</sub>	5	7	—	—	—	ns
MR Pulse Width	t <sub>w</sub>	5	—	—	—	—	ns
Recovery Time MR to CP (299)	t <sub>rec</sub>	5	—	—	—	—	ns

\*5 V: Min. is @ 4.5 V.

5 V: min. is @ 4.75 V for 0 to +70°C

## SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

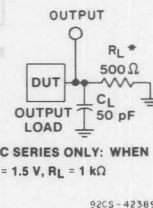
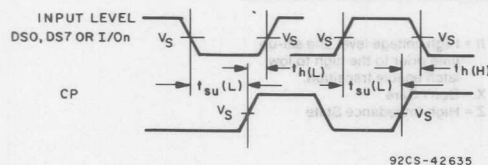
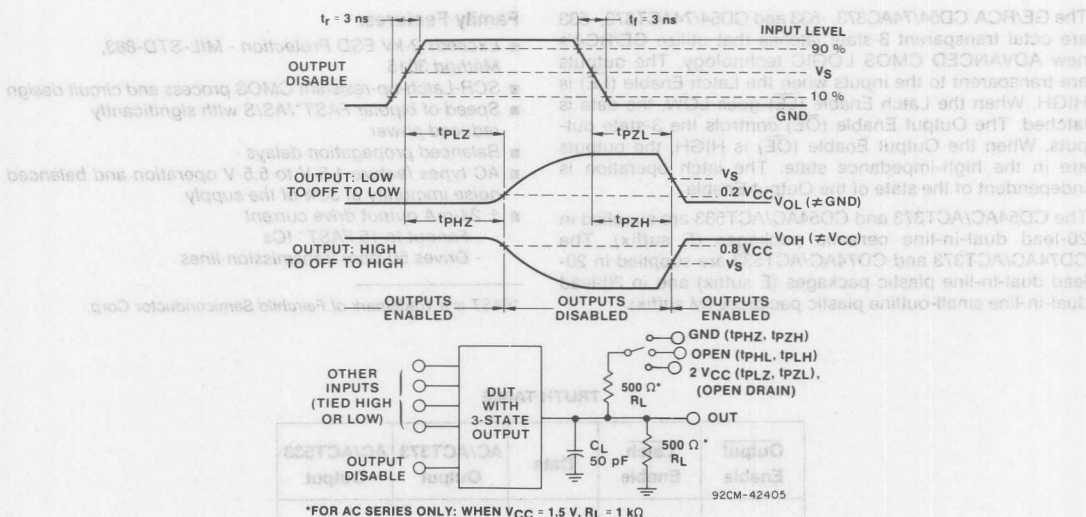
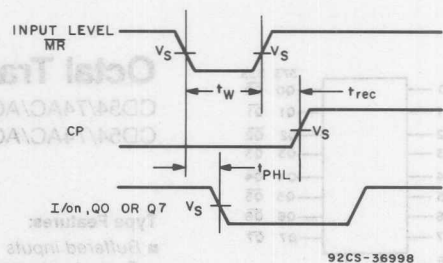
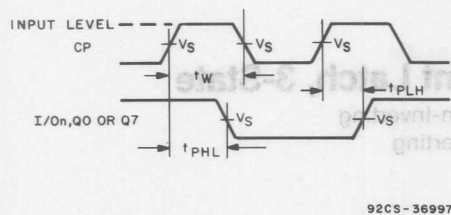
CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q0, Q7	t <sub>PLH</sub> t <sub>PHL</sub>	5*	2.3	11.5	2.2	12.9	ns
CP to (I/O)n	t <sub>PLH</sub> t <sub>PHL</sub>	5	2.6	13	2.5	14.5	ns
MR to Q0, Q7 (299 only)	t <sub>PLH</sub> t <sub>PHL</sub>	5	2.2	10.9	2.1	12.2	ns
MR to (I/O)n	t <sub>PLH</sub> t <sub>PHL</sub>	5	2.9	16.7	3.2	18.6	ns
Enable Disable Times	t <sub>PLZ</sub> t <sub>PHZ</sub> t <sub>PZL</sub> t <sub>PZH</sub>	5	2.7	13.3	2.6	14.9	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	—	—	—	—	pF
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

\*5 V: min. is @ 5.5 V  
max. is @ 4.5 V.

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

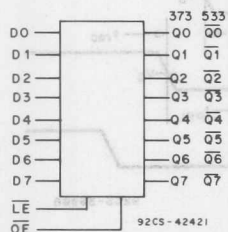
§C<sub>PD</sub> is used to determine the dynamic power consumption, per function.

$P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
f<sub>o</sub> = output frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.



	CD54/74AC	CD54/74ACT
Input Level	V <sub>CC</sub>	3 V
Input Switching Voltage, V <sub>s</sub>	0.5 V <sub>CC</sub>	1.5 V
Output Switching Voltage, V <sub>s</sub>	0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>





## Octal Transparent Latch, 3-State

CD54/74AC/ACT373 - Non-Inverting

CD54/74AC/ACT533 - Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay:  
4.3 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

### FUNCTIONAL DIAGRAM

The GE/RCA CD54/74AC373, -533 and CD54/74ACT373, -533 are octal transparent 3-state latches that utilize GE/RCA's new ADVANCED CMOS LOGIC technology. The outputs are transparent to the inputs when the Latch Enable (LE) is HIGH. When the Latch Enable (LE) goes LOW, the data is latched. The Output Enable (OE) controls the 3-state outputs. When the Output Enable (OE) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The CD54AC/ACT373 and CD54AC/ACT533 are supplied in 20-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT373 and CD74AC/ACT533 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST\* AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

### TRUTH TABLE

Output Enable	Latch Enable	Data	AC/ACT373 Output	AC/ACT533 Output
L	H	H	H	L
L	H	L	L	H
L	L	I	L	H
L	L	h	H	L
H	X	X	Z	Z

#### Note:

L = Low voltage level  
H = High voltage level  
I = Low voltage level one set-up time prior to the high to low latch enable transition

h = High voltage level one set-up time prior to the high to low latch enable transition  
X = Don't Care  
Z = High Impedance State

Output Switching Voltage, $V_o$	Input Switching Voltage, $V_i$	Input Level
0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>	V <sub>CC</sub>
1.5 V	0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>
3 V	0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>

File Number 1882

# CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 $\pm$ 1/32 in. (1.59 $\pm$ 0.79 mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

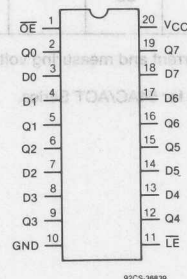
## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

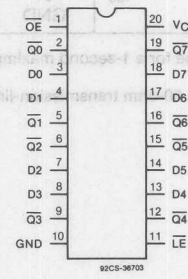
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ * (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

## TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC373, CD54/74ACT373



CD54/74AC533, CD54/74ACT533

# CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS		AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
					+25		0 to +70		-40 to +125(74)			
							-40 to +85		-55 to +125(54)			
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)	V <sub>CC</sub> (V)	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>				1.5	1.2	—	1.2	—	1.2	—	V
					3	2.1	—	2.1	—	2.1	—	
					5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V <sub>IL</sub>				1.5	—	0.3	—	0.3	—	0.3	V
					3	—	0.9	—	0.9	—	0.9	
					5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V	
			-0.05	3	2.9	—	2.9	—	2.9	—		
			-0.05	4.5	4.4	—	4.4	—	4.4	—		
			-4	3	2.58	—	2.48	—	2.4	—		
			-24	4.5	3.94	—	3.8	—	3.7	—		
			-75	5.5	—	—	3.85	—	—	—		
			-50	5.5	—	—	—	—	3.85	—		
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V	
			0.05	3	—	0.1	—	0.1	—	0.1		
			0.05	4.5	—	0.1	—	0.1	—	0.1		
			12	3	—	0.36	—	0.44	—	0.5		
			24	4.5	—	0.36	—	0.44	—	0.5		
			75	5.5	—	—	—	1.65	—	—		
			50	5.5	—	—	—	—	—	1.65		
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>									
		V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*	
	AC/ACT373	AC/ACT533
OE	0.87	0.87
Dn	0.5	0.5
LE	0.8	0.8

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

# Technical Data

## PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
LE Pulse Width	t <sub>w</sub>	1.5 3.3* 5†	75 10 6	— — —	75 10 6	— — —	ns
Setup Time Data to LE	t <sub>su</sub>	1.5 3.3 5	2 2 2	— — —	2 2 2	— — —	ns
Hold Time Data to LE	t <sub>h</sub>	1.5 3.3 5	38 5 3	— — —	38 5 3	— — —	ns

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

5 V: min is @ 4.75 V for 0 to +70°C

## SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Qn	t <sub>PLH</sub>	1.5	—	102	—	114	ns
373	t <sub>PHL</sub>	3.3*	2.7	11.5	2.6	22.3	
533		5†	1.7	8.2	1.6	9	
	t <sub>PLH</sub>	1.5	—	128	—	140	ns
	t <sub>PHL</sub>	3.3	5.1	14.3	2.9	15.8	
		5	2	10.2	1.9	11.3	
LE to Qn	t <sub>PLH</sub>	1.5	—	148	—	164	ns
373	t <sub>PHL</sub>	3.3	3.6	16.5	3.4	18.3	
533		5	2.4	11.8	2.2	13.1	
	t <sub>PLH</sub>	1.5	—	148	—	164	ns
	t <sub>PHL</sub>	3.3	3.6	16.5	3.4	18.3	
		5	2.4	11.8	2.2	13.1	
Output Enable and Disable Times	t <sub>PZL</sub>	1.5	—	162	—	181	ns
	t <sub>PZH</sub>	3.3	4.2	19.5	4.1	21.8	
	t <sub>PLZ</sub>	5	2.7	13	2.6	14.5	
Power Dissipation Capacitance	C <sub>PD</sub> §	—	90 Typ.		90 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per latch.

PD = V<sub>CC</sub><sup>2</sup> f<sub>i</sub> (C<sub>PD</sub> + C<sub>L</sub>) where f<sub>i</sub> = input frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.



# CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

## PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
LE Pulse Width	t <sub>w</sub>	5†	6	—	6	—	ns
Setup Time Data to LE	t <sub>su</sub>	5	2	—	2	—	ns
Hold Time Data to LE	t <sub>h</sub>	5	3	—	3	—	ns

†5 V: min. is @ 4.5 V  
5 V: min. is @ 4.75 V for 0 to +70°C

## SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

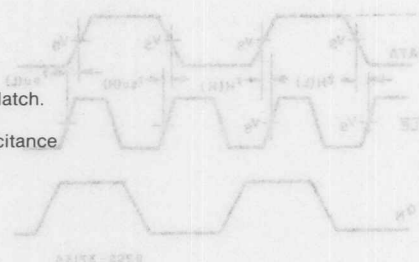
CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70° C -40 to +85° C		-40 to +125° C(74) -55 to +125° C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Qn							
373	t <sub>PLH</sub>	5†	1.6	9.4	1.5	10.4	ns
533	t <sub>PHL</sub>		2	11.4	1.8	12.7	
LE to Qn							
373	t <sub>PLH</sub>	5	2.7	13	2.6	14.5	ns
533	t <sub>PHL</sub>						
Output Enable and Disable Times	t <sub>PZL</sub> t <sub>PZH</sub> t <sub>PLZ</sub> t <sub>PHZ</sub>	5	2.7	13	2.6	14.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	108 Typ.		108 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25° C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25° C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per latch.

PD = V<sub>CC</sub><sup>2</sup> f<sub>i</sub> (C<sub>PD</sub> + C<sub>L</sub>) + V<sub>CC</sub> ΔI<sub>CC</sub> where f<sub>i</sub> = input frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.



[illegible]

- 92CS-42406

**Timing Diagram for 3-State Output Buffer**

The diagram illustrates the timing characteristics of a 3-state output buffer. The input level transitions between 90%  $V_S$  and 10%  $V_S$  (GND). The output level transitions between  $V_{OH} (\approx V_{CC})$  and  $V_{OL} (\approx 0.2 V_{CC})$  when enabled, and to a high-impedance state when disabled.

**Key Parameters:**

- $t_f = 3 \text{ ns}$ : Input signal fall time.
- $t_{PLZ}$ : Propagation delay from input low to output low.
- $t_{PZL}$ : Propagation delay from input low to output high-impedance.
- $t_{PHZ}$ : Propagation delay from input high to output high-impedance.
- $t_{PZH}$ : Propagation delay from input high to output low.
- $V_{OH} (\approx V_{CC})$ : Output high voltage level.
- $V_{OL} (\approx 0.2 V_{CC})$ : Output low voltage level.

**Circuit Diagram:**

The circuit shows the DUT with 3-state output connected to a load resistor  $R_L$  (500  $\Omega$ ) and a load capacitor  $C_L$  (50 pF). The output is also connected to a pull-up resistor  $R_L$  (500  $\Omega$ ) to  $2 V_{CC}$  (OPEN DRAIN). Other inputs are tied high or low.

92CM-42405

The diagram shows three signals: INPUT LEVEL, DATA, and QN. The DATA signal is a square wave with voltage levels 0V and  $V_S$ . The QN signal is a square wave with voltage levels 0V and  $V_S$ . The timing parameters are defined as follows:

- $t_{PLH}$ : Propagation delay from DATA rising to QN rising.
- $t_{PHL}$ : Propagation delay from DATA falling to QN falling.
- $t_{TLH}$ : Setup time before DATA rising.
- $t_{THL}$ : Hold time after DATA falling.
- 90% and 10% points are marked on the QN signal transitions.

92CS-37132

Timing diagram for the 92CS-37133. The diagram shows the relationship between the Input Level, LE (Latched Enable), DATA, and Q<sub>N</sub> (Output). The signals are shown as waveforms over time. The LE signal is a clock signal. The DATA signal is the data input. The Q<sub>N</sub> signal is the output. The timing parameters are labeled:  $t_w$  (write time),  $t_{PLH}$  (propagation delay from LE to Q<sub>N</sub>), and  $t_{PHL}$  (propagation delay from LE to Q<sub>N</sub>). The output Q<sub>N</sub> is shown as a signal that changes state when LE is high and DATA is valid. The output Q<sub>N</sub> is shown as a signal that changes state when LE is high and DATA is valid.

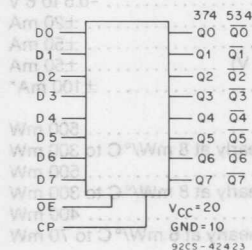
Timing diagram for the 92CS-37134. The diagram shows the relationship between the DATA input, the Latched Enable (LE) signal, and the output  $Q_N$ . The DATA signal is shown with setup and hold times relative to the LE signal. The output  $Q_N$  is shown as a square wave that changes state when the LE signal is active.

Key timing parameters shown in the diagram:

- $V_S$ : Supply voltage level.
- $t_{H(L)}$ : Hold time from the falling edge of LE to the falling edge of DATA.
- $t_{H(H)}$ : Hold time from the rising edge of LE to the rising edge of DATA.
- $t_{su(H)}$ : Setup time from the rising edge of LE to the rising edge of DATA.
- $t_{su(L)}$ : Setup time from the falling edge of LE to the falling edge of DATA.

92CS-37134

	CD54/74AC	CD54/74AC
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$



## Octal D-Type Flip-Flop, 3-State Positive-Edge Triggered

CD54/74AC/ACT374 - Non-Inverting

CD54/74AC/ACT534 - Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay:  
5 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

### FUNCTIONAL DIAGRAM

The GE/RCA-CD54/74AC374, -534 and CD54/74ACT374, -534 are octal D-type, 3-state, positive-edge-triggered flip-flops that utilize GE/RCA's new ADVANCED CMOS LOGIC technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable ( $\overline{OE}$ ) controls the 3-state outputs and is independent of the register operation. When the Output Enable ( $\overline{OE}$ ) is HIGH, the outputs are in the high-impedance state. The CD54/74AC/ACT374 and CD54/74AC/ACT534 share the same pin configurations, but the CD54/74AC/ACT374 outputs are non-inverted while the CD54/74AC/ACT534 devices have inverted outputs. (For flow-through pin configurations, see CD54/74AC/ACT564 and CD54/74AC/ACT574.)

The CD54AC/ACT374 and CD54AC/ACT534 are supplied in 20-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT374 and CD74AC/ACT534 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

### TRUTH TABLE

INPUTS			OUTPUTS	
			374 Qn	534 $\overline{Qn}$
$\overline{OE}$	CP	Dn		
L		H	H	L
L		L	L	H
L	L	X	Qo	$\overline{Qo}$
H	X	X	Z	Z

H = High level (steady state)

L = Low level (steady state)

X = Don't care

= Transition from low to high level

Qo = The level of Q before the indicated steady-state input conditions were established

Z = High impedance

# CD54/74AC374, CD54/74AC534 CD54/74ACT374, CD54/74ACT534

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*

## POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW

## OPERATING-TEMPERATURE RANGE ( $T_A$ ):

PACKAGE TYPE F	$-55$ to $+125^\circ\text{C}$
PACKAGE TYPE E, M	$-40$ to $+125^\circ\text{C}$

## STORAGE TEMPERATURE ( $T_{stg}$ )

$-65$  to  $+150^\circ\text{C}$

## LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

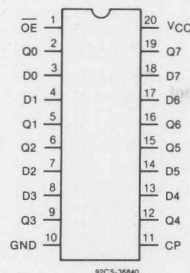
## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

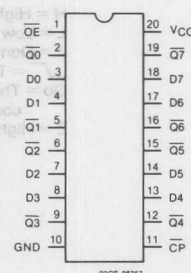
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *, (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40 -55	+125 +125	$^\circ\text{C}$ $^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

## TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT374



CD54/74AC/ACT534

# CD54/74AC374, CD54/74AC534

## CD54/74ACT374, CD54/74ACT534

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS				TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
							+25		0 to +70		-40 to +125(74)			
									-40 to +85		-55 to +125(54)			
				V <sub>I</sub> (V)	I <sub>O</sub> (mA)	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	—	2	V <sub>IH</sub>	—	—	1.5	1.2	—	1.2	—	1.2	—	V	
						3	2.1	—	2.1	—	2.1	—		
						5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage	—	4.5	V <sub>IL</sub>	—	0.0	1.5	—	0.3	—	0.3	—	0.3	V	
						3	—	0.9	—	0.9	—	0.9		
						5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage	—	0.1	V <sub>OH</sub>	—	-0.05	1.5	1.4	—	1.4	—	1.4	—	V	
						3	2.9	—	2.9	—	2.9	—		
						4.5	4.4	—	4.4	—	4.4	—		
						3	2.58	—	2.48	—	2.4	—		
						4.5	3.94	—	3.8	—	3.7	—		
						5.5	—	—	3.85	—	—	—		
						5.5	—	—	—	—	3.85	—		
Low-Level Output Voltage	—	0.1	V <sub>OL</sub>	—	0.05	1.5	—	0.1	—	0.1	—	0.1	V	
						3	—	0.1	—	0.1	—	0.1		
						4.5	—	0.1	—	0.1	—	0.1		
						12	3	—	0.36	—	0.44	—		0.5
						24	4.5	—	0.36	—	0.44	—		0.5
						75	5.5	—	—	1.65	—	—		
						50	5.5	—	—	—	—	1.65		
Input Leakage Current	—	—	I <sub>I</sub>	V <sub>CC</sub> or GND	—	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	—	—	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>	—	—	—	—	—	—	—	—	μA	
				V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	±0.5	—	±5	—	±10			
Quiescent Supply Current, MSI	—	—	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.



# STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS
		$V_I$ (V)	$I_O$ (mA)		+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	$V_{IH}$	—	—	4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	$V_{IL}$	—	—	4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$ # *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$ # *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	$I_I$	$V_{CC}$ or GND	—	5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	$I_{OZ}$	$V_{IH}$ or $V_{IL}$ $V_O = V_{CC}$ or GND	—	—	—	—	—	—	—	—	μA
			—	—	—	—	—	—	—	—	
			5.5	—	±0.5	—	±5	—	±10		
			—	—	—	—	—	—	—		
Quiescent Supply Current, MSI	$I_{CC}$	$V_{CC}$ or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	$\Delta I_{CC}$	$V_{CC}-2.1$	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

## ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
D, OE	0.7
CP	1.17

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

# PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width	t <sub>w</sub>	1.5 3.3* 5†	75 11 5.9	— — —	85 12 6.7	— — —	ns
Setup Time Data to Clock	t <sub>su</sub>	1.5 3.3 5	2 2 2	— — —	2 2 2	— — —	ns
Hold Time Data to Clock	t <sub>h</sub>	1.5 3.3 5	2 2 2	— — —	2 2 2	— — —	ns
Maximum Clock Frequency	f <sub>MAX</sub>	1.5 3.3 5	6.5 48 85	— — —	6 42 75	— — —	MHz

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

5 V: min is @ 4.75 V for 0 to +70°C

## SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Clock to Q AC374	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3* 5†	— 3 2	125 14 10	— 2.8 1.8	135 15.1 10.8	ns
Clock to $\bar{Q}$ AC534	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 3.1 2	128 14.3 10.2	— 2.9 1.9	140 15.8 11.3	ns
Output Enable and Disable to Q AC374	t <sub>PLZ</sub> t <sub>PHZ</sub> t <sub>PZL</sub> t <sub>PZH</sub>	1.5 3.3 5	— 4.2 2.7	162 19.5 13	— 4.1 2.6	181 24.8 14.5	ns
Output Enable and Disable to $\bar{Q}$ AC534	t <sub>PLZ</sub> t <sub>PHZ</sub> t <sub>PZL</sub> t <sub>PZH</sub>	1.5 3.3 5	— 4.2 2.7	162 19.5 13	— 4.1 2.6	181 24.8 14.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	60 Typ.		60 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V

max. is @ 3 V

†5 V: min. is @ 5.5 V

max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C

max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per flip flop.

PD = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>i</sub> +  $\Sigma$  V<sub>CC</sub><sup>2</sup> f<sub>o</sub> C<sub>L</sub> where f<sub>i</sub> = input frequency

f<sub>o</sub> = output frequency

C<sub>L</sub> = output load capacitance

V<sub>CC</sub> = supply voltage.

# Technical Data

## CD54/74AC374, CD54/74AC534 CD54/74ACT374, CD54/74ACT534

### PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width	t <sub>w</sub>	5†	6.7	—	7.4	—	ns
Setup Time Data to Clock	t <sub>SU</sub>	5	2	—	2	—	ns
Hold Time Data to Clock	t <sub>H</sub>	5	3	—	3	—	ns
Maximum Clock Frequency	f <sub>MAX</sub>	5	75	—	68	—	MHz

†5 V: min. is @ 4.5 V

5 V: min. is @ 4.75 V for 0 to +70°C

### SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70° C -40 to +85° C		-40 to +125° C(74) -55 to +125° C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
Clock to Q ACT374	t <sub>PLH</sub> t <sub>PHL</sub>	5†	2.1	10.3	1.9	11.2	ns
Clock to Q̄ ACT534	t <sub>PLH</sub> t <sub>PHL</sub>	5	2.1	10.6	2	11.7	ns
Output Enable and Disable to Q ACT374	t <sub>PLZ</sub> t <sub>PHZ</sub> t <sub>PZL</sub> t <sub>PZH</sub>	5	2.7	13	2.6	14.5	ns
Output Enable and Disable to Q̄ ACT534	t <sub>PLZ</sub> t <sub>PHZ</sub> t <sub>PZL</sub> t <sub>PZH</sub>	5	2.7	13	2.6	14.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	60 Typ.		60 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25° C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25° C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per flip flop.

PD = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup> f<sub>i</sub> + V<sub>CC</sub><sup>2</sup> f<sub>o</sub> C<sub>L</sub> + V<sub>CC</sub> ΔI<sub>CC</sub> where f<sub>i</sub> = input frequency  
f<sub>o</sub> = output frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.

# CD54/74AC374, CD54/74AC534 CD54/74ACT374, CD54/74ACT534

## PARAMETER MEASUREMENT INFORMATION

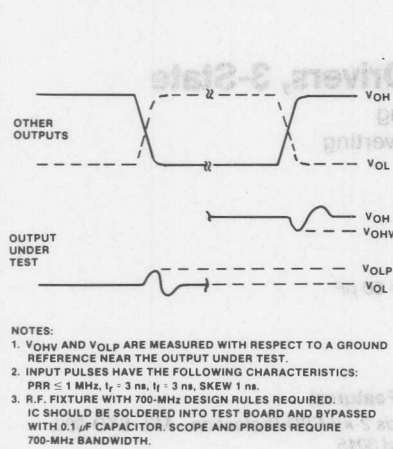


Fig. 1 - Simultaneous switching transient waveforms.

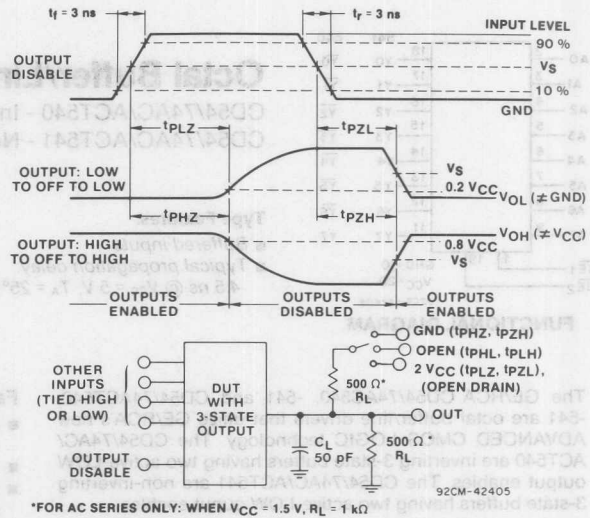


Fig. 2 - Three-state propagation delay waveforms and test circuit.

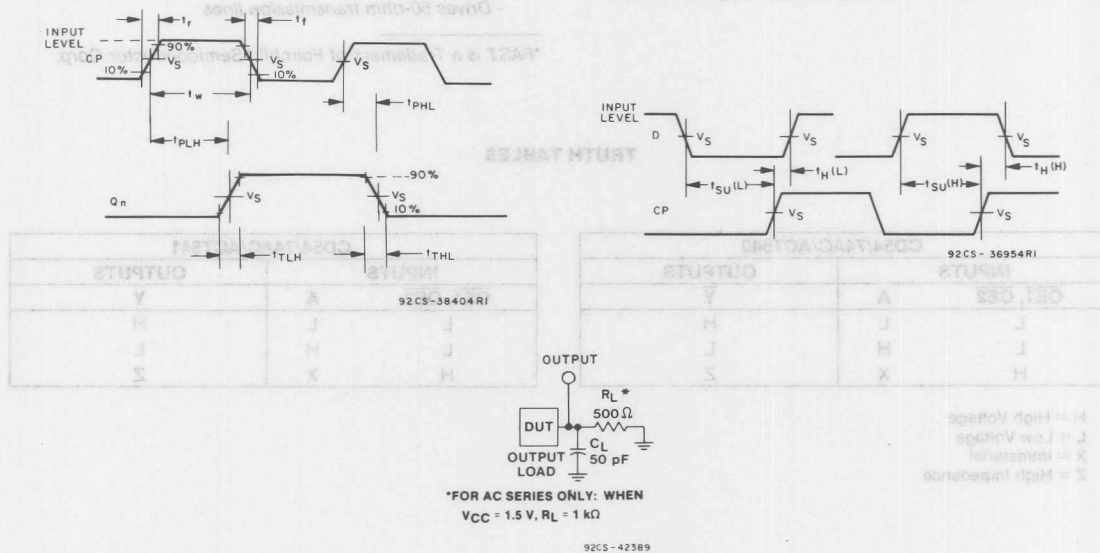
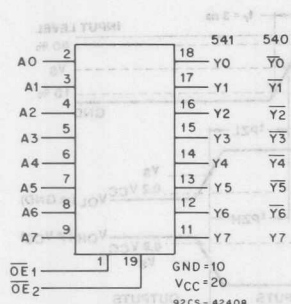


Fig. 3 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$



### FUNCTIONAL DIAGRAM

The GE/RCA CD54/74AC540, -541 and CD54/74ACT540, -541 are octal buffer/line drivers that utilize GE/RCA's new ADVANCED CMOS LOGIC technology. The CD54/74AC/ACT540 are inverting 3-state buffers having two active-LOW output enables. The CD54/74AC/ACT541 are non-inverting 3-state buffers having two active-LOW output enables.

The CD54AC540, -541 and CD54ACT540, -541 are supplied in 20-lead dual-in-line ceramic packages (F suffix). The CD74AC540, -541 and CD74ACT540, -541 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix).

## Octal Buffer/Line Drivers, 3-State

CD54/74AC/ACT540 - Inverting

CD54/74AC/ACT541 - Non-Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay:  
4.5 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

### TRUTH TABLES

CD54/74AC/ACT540		
INPUTS		OUTPUTS
OE1, OE2	A	$\bar{Y}$
L	L	H
L	H	L
H	X	Z

CD54/74AC/ACT541		
INPUTS		OUTPUTS
OE1, OE2	A	Y
L	L	H
L	H	L
H	X	Z

H = High Voltage  
L = Low Voltage  
X = Immaterial  
Z = High Impedance

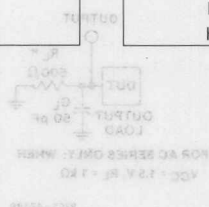


Fig. 3 - Propagation delay times and test circuit

CD54/74AC	CD54/74ACT	CD54/74M
3 V	3 V	3 V
1.5 V	1.5 V	1.5 V
0.5 V	0.5 V	0.5 V

File Number 1857



# **MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

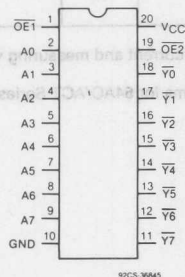
## **RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

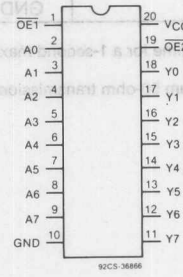
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ :			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

## **TERMINAL ASSIGNMENT DIAGRAMS**



CD54/74AC/ACT540



CD54/74AC/ACT541

# CD54/74AC540, CD54/74AC541 CD54/74ACT540, CD54/74ACT541

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
						+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V		
			3	2.1	—	2.1	—	2.1	—			
			5.5	3.85	—	3.85	—	3.85	—			
Low-Level Input Voltage V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V		
			3	—	0.9	—	0.9	—	0.9			
			5.5	—	1.65	—	1.65	—	1.65			
High-Level Output Voltage V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V		
		-0.05	3	2.9	—	2.9	—	2.9	—			
		-0.05	4.5	4.4	—	4.4	—	4.4	—			
		-4	3	2.58	—	2.48	—	2.4	—			
		-24	4.5	3.94	—	3.8	—	3.7	—			
		-75	5.5	—	—	3.85	—	—	—			
		-50	5.5	—	—	—	—	3.85	—			
Low-Level Output Voltage V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V		
		0.05	3	—	0.1	—	0.1	—	0.1			
		0.05	4.5	—	0.1	—	0.1	—	0.1			
		12	3	—	0.36	—	0.44	—	0.5			
		24	4.5	—	0.36	—	0.44	—	0.5			
		75	5.5	—	—	—	1.65	—	—			
		50	5.5	—	—	—	—	—	1.65			
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# CD54/74AC540, CD54/74AC541 CD54/74ACT540, CD54/74ACT541

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS		
			+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	$V_{IH}$	4.5 to 5.5	2	—	2	—	2	—	V		
Low-Level Input Voltage	$V_{IL}$	4.5 to 5.5	—	0.8	—	0.8	—	0.8	V		
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	4.5	4.4	—	4.4	—	4.4	—	
		#	-24	4.5	3.94	—	3.8	—	3.7	—	
		*	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.05	4.5	—	0.1	—	0.1	—	0.1	
		#	24	4.5	—	0.36	—	0.44	—	0.5	
		*	75	5.5	—	—	—	1.65	—	—	
		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	$I_I$	$V_{CC}$ or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	$I_{OZ}$	$V_{IH}$ or $V_{IL}$	—	—	—	—	—	—	—	—	
		$V_{IL}$ or $V_{CC}$	5.5	—	±0.5	—	±5	—	±10	μA	
		$V_{CC}$ or GND	—	—	—	—	—	—	—	—	
Quiescent Supply Current, MSI	$I_{CC}$	$V_{CC}$ or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	$\Delta I_{CC}$	$V_{CC}$ -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

### ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*	
	540	541
DATA	1.42	0.5
OE1, OE2	1.3	1.3

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

# Technical Data

## CD54/74AC540, CD54/74AC541 CD54/74ACT540, CD54/74ACT541

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output AC540	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3* 5†	— 2.2 1.3	85 9.2 6.6	— 2.1 1.3	95 10.6 7.6	ns
AC541	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 2.8 1.8	108 12 8.6	— 2.7 1.7	120 13.4 9.6	ns
Enable, Disable to Output	t <sub>PZL</sub> t <sub>PLZ</sub> t <sub>PZH</sub> t <sub>PHZ</sub>	1.5 3.3 5	— 3.9 2.5	150 18 12	— 3.8 2.4	167 20.1 13.4	ns
Power Dissipation Capacitance AC540 AC541	C <sub>PD</sub> §	— —	95 Typ. 80 Typ.		95 Typ. 80 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output ACT540	t <sub>PLH</sub> t <sub>PHL</sub>	5†	1.6	8	1.5	8.9	ns
ACT541	t <sub>PLH</sub> t <sub>PHL</sub>	5†	2	9.8	1.9	11	ns
Enable, Disable to Output	t <sub>PLZ</sub> t <sub>PLZL</sub> t <sub>PZH</sub> t <sub>PHZ</sub>	5	2.7	13.2	2.5	14.7	ns
Power Dissipation Capacitance ACT540 ACT541	C <sub>PD</sub> §	— —	115 Typ. 100 Typ.		115 Typ. 100 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

$\$C_{PD}$  is used to determine the dynamic power consumption, per channel.

For AC series,  $PD = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT series,  $PD = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where

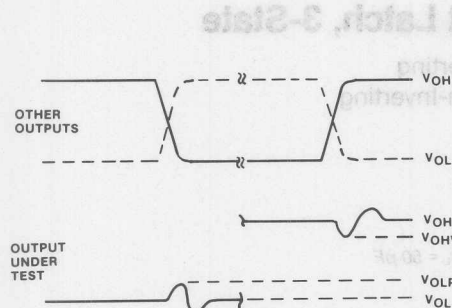
$f_i$  = input frequency

$C_L$  = output load capacitance

$V_{CC}$  = supply voltage.

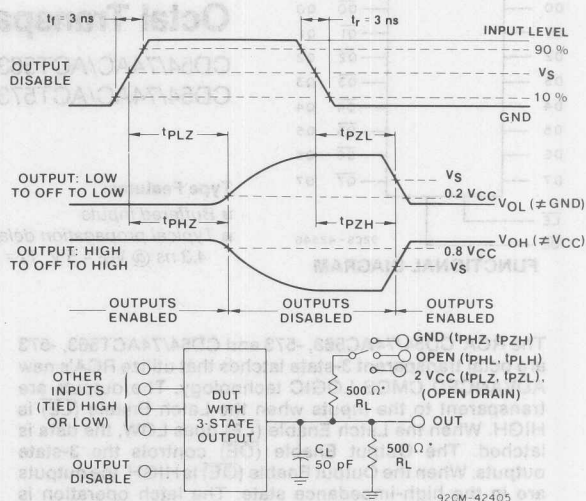
$t_f = 3 \text{ ns}$

## OTHER OUTPUTS



- NOTES:
1.  $V_{OH}$  AND  $V_{OL}$  ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:  
 $PRR \leq 1$  MHz,  $t_r = 3$  ns,  $t_f = 3$  ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.  
IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1  $\mu$ F CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406



\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

Fig. 2 - Three-state propagation delay waveforms and test circuit.

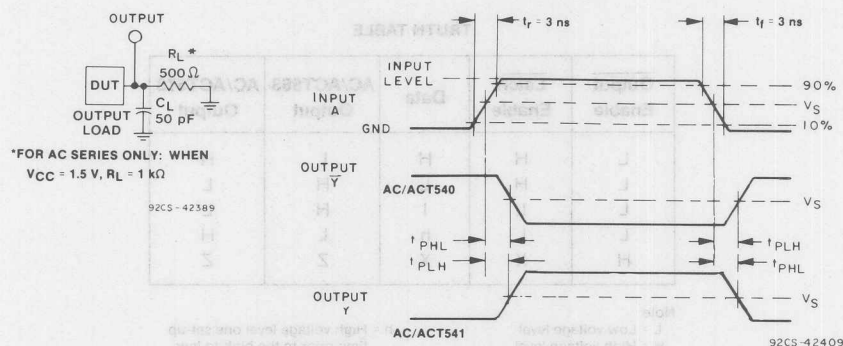
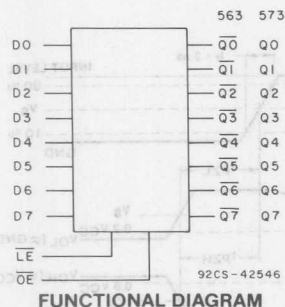


Fig. 3 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_s$	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, $V_s$	$0.5 V_{CC}$	$0.5 V_{CC}$





## Octal Transparent Latch, 3-State

CD54/74AC/ACT563 - Inverting

CD54/74AC/ACT573 - Non-Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay:  
4.3 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{ C}$ ,  $C_L = 50\text{ pF}$

The RCA CD54/74AC563, -573 and CD54/74ACT563, -573 are octal transparent 3-state latches that utilize RCA's new ADVANCED CMOS LOGIC technology. The outputs are transparent to the inputs when the Latch Enable (LE) is HIGH. When the Latch Enable (LE) goes LOW, the data is latched. The Output Enable (OE) controls the 3-state outputs. When the Output Enable (OE) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The CD54AC/ACT563 and CD54AC/ACT573 are supplied in 20-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT563 and CD74AC/ACT573 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

Output Enable	Latch Enable	Data	AC/ACT563 Output	AC/ACT573 Output
L	H	H	L	H
L	H	L	H	L
L	L	I	H	L
L	L	h	L	H
H	X	X	Z	Z

Note:

L = Low voltage level  
H = High voltage level  
I = Low voltage level one set-up time prior to the high to low latch enable transition

h = High voltage level one set-up time prior to the high to low latch enable transition.  
X = Don't Care  
Z = High Impedance State

CD54/74AC/ACT563	CD54/74AC/ACT573	Input Level
3V	3V	Input Switching Voltage $V_i$
1.5V	0.8V	Output Switching Voltage $V_o$
0.8V	0.5V	

File Number 1956

# CD54/74AC563, CD54/74AC573 CD54/74ACT563, CD54/74ACT573

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ OR GROUND CURRENT ( $I_{CC}$ OR $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

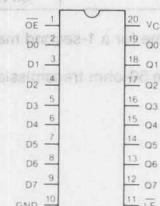
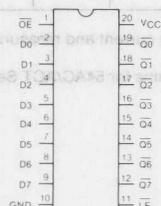
## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ :( (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I, V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V(AC Types) at 3.6 V to 5.5 V(AC Types) at 4.5 V to 5.5 V(ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

## TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC563, CD54/74ACT563

CD54/74AC573, CD54/74ACT573

# CD54/74AC563, CD54/74AC573 CD54/74ACT563, CD54/74ACT573

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
						+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V	
				3	2.1	—	2.1	—	2.1	—		
				5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage	V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3		
				3	—	0.9	—	0.9	—	0.9	V	
				5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub>	-0.05	1.5	1.4	—	1.4	—	1.4	—		
			-0.05	3	2.9	—	2.9	—	2.9	—		
		or	-0.05	4.5	4.4	—	4.4	—	4.4	—		
		V <sub>IL</sub>	-4	3	2.58	—	2.48	—	2.4	—	V	
			-24	4.5	3.94	—	3.8	—	3.7	—		
		#	-75	5.5	—	—	3.85	—	—	—		
		*	-50	5.5	—	—	—	—	3.85	—		
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub>	0.05	1.5	—	0.1	—	0.1	—	0.1		
			0.05	3	—	0.1	—	0.1	—	0.1		
		or	0.05	4.5	—	0.1	—	0.1	—	0.1		
		V <sub>IL</sub>	12	3	—	0.36	—	0.44	—	0.5	V	
			24	4.5	—	0.36	—	0.44	—	0.5		
		#	75	5.5	—	—	—	1.65	—	—		
		*	50	5.5	—	—	—	—	—	1.65		
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	25					
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.			
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	— V
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8 V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	-0.05	4.5	4.4	—	4.4	—	4.4	— V
			-24	4.5	3.94	—	3.8	—	3.7	—
			-75	5.5	—	—	3.85	—	—	—
			-50	5.5	—	—	—	—	3.85	—
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> # *	0.05	4.5	—	0.1	—	0.1	—	0.1 V
			24	4.5	—	0.36	—	0.44	—	0.5
			75	5.5	—	—	—	1.65	—	—
			50	5.5	—	—	—	—	—	1.65
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1 μA
3-State Leakage Current	I <sub>oz</sub>	V <sub>IH</sub> or V <sub>IL</sub>								
		V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10 μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160 μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3 mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*	
	ACT563	ACT573
OE	0.87	0.87
Dn	0.5	0.5
LE	0.8	0.8

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

		$V_{CC}$ (V)	(54)				UNITS
			MIN.	MAX.	MIN.	MAX.	
	$t_w$	1.5 3.3* 5†	75 10 6	— — —	75 10 6	— — —	ns
Setup Data to $\overline{LE}$	$t_{su}$	1.5 3.3 5	2 2 2	— — —	2 2 2	— — —	ns
Hold Time Data to $\overline{LE}$	$t_h$	1.5 3.3 5	38 5 3	— — —	38 5 3	— — —	ns

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

5 V: min is @ 4.75 V for 0 to +70°C

**SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3$  ns,  $C_L = 50$  pF**

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70° C -40 to +85° C		-40 to +125° C (74) -55 to +125° C (54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Qn AC563	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 5.1 2	128 14.3 10.2	— 2.9 1.9	140 15.8 11.3	ns
AC573	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3* 5†	— 2.7 1.7	102 11.5 8.2	— 2.6 1.6	114 12.6 9	ns
$\overline{LE}$ on Qn AC563	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 3.6 2.4	148 16.5 11.8	— 3.4 2.2	164 18.3 13.1	ns
AC573	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 3.6 2.4	148 16.5 11.8	— 3.4 2.2	164 18.3 13.1	ns
Output Enable and Disable Times	t <sub>PZL</sub> t <sub>PZH</sub> t <sub>PLZ</sub> t <sub>PHZ</sub>	1.5 3.3 5	— 4.2 2.7	162 19.5 13	— 4.1 2.6	181 21.8 14.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	90 Typ.		90 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25° C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25° C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

$\S C_{PD}$  is used to determine the dynamic power consumption, per latch.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency

$C_L$  = output load capacitance

$V_{CC}$  = supply voltage.



# CD54/74AC563, CD54/74AC573

## CD54/74ACT563, CD54/74ACT573

## PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
LE Pulse Width	t <sub>w</sub>	5†	6	—	6	—	ns
Setup Time Data to LE	t <sub>su</sub>	5	2	—	2	—	ns
Hold Time Data to LE	t <sub>h</sub>	5	3	—	3	—	ns

†5 V: min. is @ 4.5 V

5 V: min. is @ 4.75 V for 0 to +70°C

SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Qn	t <sub>PLH</sub> t <sub>PHL</sub>	5†	2	11.4	1.8	12.7	ns
563			1.6	9.4	1.5	10.4	
573							
LE to Qn	t <sub>PLH</sub> t <sub>PHL</sub>	5	2.7	13	2.6	14.5	ns
563							
573							
Output Enable and Disable Times	t <sub>PZL</sub> t <sub>PZH</sub> t <sub>PLZ</sub> t <sub>PHZ</sub>	5	2.7	13	2.6	14.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	108 Typ.		108 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V

max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C

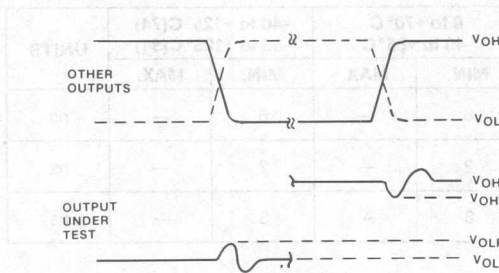
max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per latch.P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> f<sub>i</sub> (C<sub>PD</sub> + C<sub>L</sub>) + V<sub>CC</sub>ΔI<sub>CC</sub> where f<sub>i</sub> = input frequencyC<sub>L</sub> = output load capacitanceV<sub>CC</sub> = supply voltage.

Input Level	Output Level	Input Switching Voltage	Output Switching Voltage
5 V	5 V	5 V	5 V
5 V	0 V	5 V	0 V
0 V	5 V	0 V	5 V
0 V	0 V	0 V	0 V

# CD54/74AC563, CD54/74AC573 CD54/74ACT563, CD54/74ACT573

## PARAMETER MEASUREMENT INFORMATION

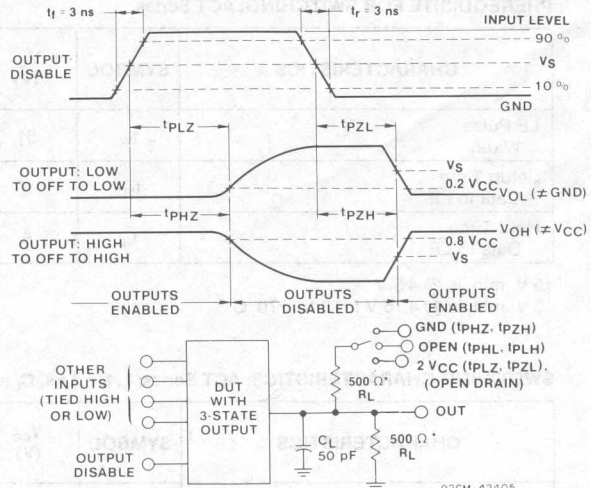


### NOTES:

1.  $V_{OHV}$  and  $V_{OLP}$  ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:  
PRR = 1 MHz,  $t_r = 3$  ns,  $t_f = 3$  ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.  
IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1  $\mu$ F CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

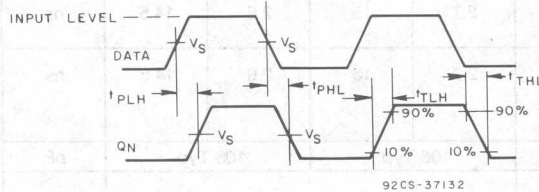
92CS-4240E

Fig. 1 - Simultaneous switching transient waveforms.



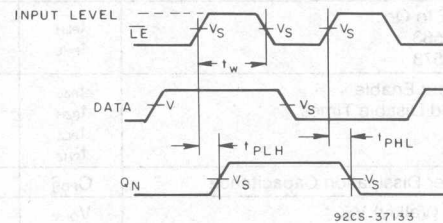
\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5$  V,  $R_L = 1$  k $\Omega$

Fig. 2 - Three-state propagation delay waveforms and test circuit.



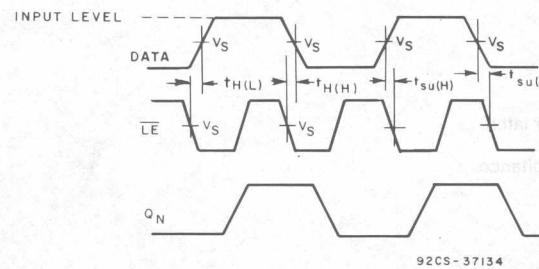
92CS-37132

Fig. 3 - Data to Qn output propagation delays.



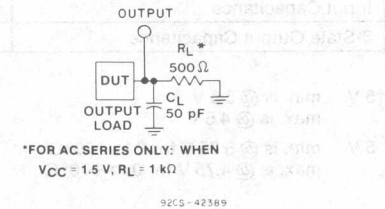
92CS-37133

Fig. 4 - Latch enable propagation delays.



92CS-37134

Fig. 5 - Latch enable prerequisite times.



\*FOR AC SERIES ONLY: WHEN  
 $V_{CC} = 1.5$  V,  $R_L = 1$  k $\Omega$

Fig. 6 - Test circuit.

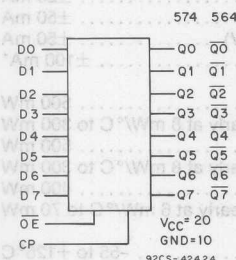
	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$

Advance Information

# CD54/74AC564, CD54/74AC574 CD54/74ACT564, CD54/74ACT574

## Octal D-Type Flip-Flop, 3-State Positive-Edge-Triggered

CD54/74AC/ACT564 - Inverting  
CD54/74AC/ACT574 - Non-Inverting



FUNCTIONAL DIAGRAM

### Type Features:

- Buffered inputs
- Typical propagation delay:  
6.5 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

The GE/RCA-CD54/74AC564, -574 and CD54/74ACT564, -574 are octal D-type, 3-state, positive-edge-triggered flip-flops that utilize GE/RCA's new ADVANCED CMOS LOGIC technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable ( $\overline{OE}$ ) controls the 3-state outputs and is independent of the register operation. When the Output Enable ( $\overline{OE}$ ) is HIGH, the outputs are in the high-impedance state. The CD54/74AC/ACT564 and CD54/74AC/ACT574 share the same pin configurations, but the CD54/74AC/ACT564 outputs are inverted while the CD54/74AC/ACT574 outputs are non-inverted.

The CD54AC/ACT564 and CD54AC/ACT574 are supplied in 20-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT564 and CD74AC/ACT574 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

V <sub>CC</sub>	V <sub>OH</sub>	V <sub>OL</sub>	INPUTS		OUTPUTS	
			$\overline{OE}$	CP	564 $\overline{Q_n}$	574 $Q_n$
5.0	2.0	0	L	—	L	H
5.0	2.0	0	L	—	H	L
5.0	2.0	0	L	L	X	X
5.0	2.0	0	L	H	X	X
5.0	2.0	0	H	—	Z	Z

H = High level (steady state)

L = Low level (steady state)

X = Don't care

— = Transition from low to high level

$Q_0$  = The level of Q before the indicated steady-state input conditions were established

$\overline{Q_0}$  = The level of  $\overline{Q}$  before the indicated steady-state input conditions were established.

Z = High impedance

CD54/74AC564, CD54/74AC574  
CD54/74ACT564, CD54/74ACT574

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ OR GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 $\pm$ 1/32 in. (1.59 $\pm$ 0.79 mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

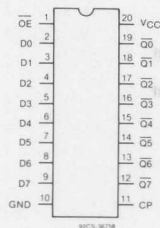
RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

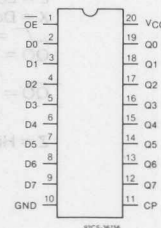
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT564



CD54/74AC/ACT574

# STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
				+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V <sub>IH</sub>		1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V	
Low-Level Input Voltage	V <sub>IL</sub>		1.5 3 5.5	— 0.9 1.65	0.3 — —	— 0.9 1.65	0.3 — —	— 0.9 1.65	0.3 — 1.65	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I <sub>oz</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>OC</sub> = V <sub>CC</sub> or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

UNIT LOADS	INPUT
1.0	0.05
1.1	0.1

\*Unit load is 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.  
Characteristic Class: 74, 54, 74C, 54C, 74F, 54F, 74V, 54V, 74VC, 54VC, 74VCT, 54VCT, 74VCT1, 54VCT1, 74VCT2, 54VCT2, 74VCT3, 54VCT3, 74VCT4, 54VCT4, 74VCT5, 54VCT5, 74VCT6, 54VCT6, 74VCT7, 54VCT7, 74VCT8, 54VCT8, 74VCT9, 54VCT9, 74VCT10, 54VCT10, 74VCT11, 54VCT11, 74VCT12, 54VCT12, 74VCT13, 54VCT13, 74VCT14, 54VCT14, 74VCT15, 54VCT15, 74VCT16, 54VCT16, 74VCT17, 54VCT17, 74VCT18, 54VCT18, 74VCT19, 54VCT19, 74VCT20, 54VCT20, 74VCT21, 54VCT21, 74VCT22, 54VCT22, 74VCT23, 54VCT23, 74VCT24, 54VCT24, 74VCT25, 54VCT25, 74VCT26, 54VCT26, 74VCT27, 54VCT27, 74VCT28, 54VCT28, 74VCT29, 54VCT29, 74VCT30, 54VCT30, 74VCT31, 54VCT31, 74VCT32, 54VCT32, 74VCT33, 54VCT33, 74VCT34, 54VCT34, 74VCT35, 54VCT35, 74VCT36, 54VCT36, 74VCT37, 54VCT37, 74VCT38, 54VCT38, 74VCT39, 54VCT39, 74VCT40, 54VCT40, 74VCT41, 54VCT41, 74VCT42, 54VCT42, 74VCT43, 54VCT43, 74VCT44, 54VCT44, 74VCT45, 54VCT45, 74VCT46, 54VCT46, 74VCT47, 54VCT47, 74VCT48, 54VCT48, 74VCT49, 54VCT49, 74VCT50, 54VCT50, 74VCT51, 54VCT51, 74VCT52, 54VCT52, 74VCT53, 54VCT53, 74VCT54, 54VCT54, 74VCT55, 54VCT55, 74VCT56, 54VCT56, 74VCT57, 54VCT57, 74VCT58, 54VCT58, 74VCT59, 54VCT59, 74VCT60, 54VCT60, 74VCT61, 54VCT61, 74VCT62, 54VCT62, 74VCT63, 54VCT63, 74VCT64, 54VCT64, 74VCT65, 54VCT65, 74VCT66, 54VCT66, 74VCT67, 54VCT67, 74VCT68, 54VCT68, 74VCT69, 54VCT69, 74VCT70, 54VCT70, 74VCT71, 54VCT71, 74VCT72, 54VCT72, 74VCT73, 54VCT73, 74VCT74, 54VCT74, 74VCT75, 54VCT75, 74VCT76, 54VCT76, 74VCT77, 54VCT77, 74VCT78, 54VCT78, 74VCT79, 54VCT79, 74VCT80, 54VCT80, 74VCT81, 54VCT81, 74VCT82, 54VCT82, 74VCT83, 54VCT83, 74VCT84, 54VCT84, 74VCT85, 54VCT85, 74VCT86, 54VCT86, 74VCT87, 54VCT87, 74VCT88, 54VCT88, 74VCT89, 54VCT89, 74VCT90, 54VCT90, 74VCT91, 54VCT91, 74VCT92, 54VCT92, 74VCT93, 54VCT93, 74VCT94, 54VCT94, 74VCT95, 54VCT95, 74VCT96, 54VCT96, 74VCT97, 54VCT97, 74VCT98, 54VCT98, 74VCT99, 54VCT99, 74VCT100, 54VCT100, 74VCT101, 54VCT101, 74VCT102, 54VCT102, 74VCT103, 54VCT103, 74VCT104, 54VCT104, 74VCT105, 54VCT105, 74VCT106, 54VCT106, 74VCT107, 54VCT107, 74VCT108, 54VCT108, 74VCT109, 54VCT109, 74VCT110, 54VCT110, 74VCT111, 54VCT111, 74VCT112, 54VCT112, 74VCT113, 54VCT113, 74VCT114, 54VCT114, 74VCT115, 54VCT115, 74VCT116, 54VCT116, 74VCT117, 54VCT117, 74VCT118, 54VCT118, 74VCT119, 54VCT119, 74VCT120, 54VCT120, 74VCT121, 54VCT121, 74VCT122, 54VCT122, 74VCT123, 54VCT123, 74VCT124, 54VCT124, 74VCT125, 54VCT125, 74VCT126, 54VCT126, 74VCT127, 54VCT127, 74VCT128, 54VCT128, 74VCT129, 54VCT129, 74VCT130, 54VCT130, 74VCT131, 54VCT131, 74VCT132, 54VCT132, 74VCT133, 54VCT133, 74VCT134, 54VCT134, 74VCT135, 54VCT135, 74VCT136, 54VCT136, 74VCT137, 54VCT137, 74VCT138, 54VCT138, 74VCT139, 54VCT139, 74VCT140, 54VCT140, 74VCT141, 54VCT141, 74VCT142, 54VCT142, 74VCT143, 54VCT143, 74VCT144, 54VCT144, 74VCT145, 54VCT145, 74VCT146, 54VCT146, 74VCT147, 54VCT147, 74VCT148, 54VCT148, 74VCT149, 54VCT149, 74VCT150, 54VCT150, 74VCT151, 54VCT151, 74VCT152, 54VCT152, 74VCT153, 54VCT153, 74VCT154, 54VCT154, 74VCT155, 54VCT155, 74VCT156, 54VCT156, 74VCT157, 54VCT157, 74VCT158, 54VCT158, 74VCT159, 54VCT159, 74VCT160, 54VCT160, 74VCT161, 54VCT161, 74VCT162, 54VCT162, 74VCT163, 54VCT163, 74VCT164, 54VCT164, 74VCT165, 54VCT165, 74VCT166, 54VCT166, 74VCT167, 54VCT167, 74VCT168, 54VCT168, 74VCT169, 54VCT169, 74VCT170, 54VCT170, 74VCT171, 54VCT171, 74VCT172, 54VCT172, 74VCT173, 54VCT173, 74VCT174, 54VCT174, 74VCT175, 54VCT175, 74VCT176, 54VCT176, 74VCT177, 54VCT177, 74VCT178, 54VCT178, 74VCT179, 54VCT179, 74VCT180, 54VCT180, 74VCT181, 54VCT181, 74VCT182, 54VCT182, 74VCT183, 54VCT183, 74VCT184, 54VCT184, 74VCT185, 54VCT185, 74VCT186, 54VCT186, 74VCT187, 54VCT187, 74VCT188, 54VCT188, 74VCT189, 54VCT189, 74VCT190, 54VCT190, 74VCT191, 54VCT191, 74VCT192, 54VCT192, 74VCT193, 54VCT193, 74VCT194, 54VCT194, 74VCT195, 54VCT195, 74VCT196, 54VCT196, 74VCT197, 54VCT197, 74VCT198, 54VCT198, 74VCT199, 54VCT199, 74VCT200, 54VCT200, 74VCT201, 54VCT201, 74VCT202, 54VCT202, 74VCT203, 54VCT203, 74VCT204, 54VCT204, 74VCT205, 54VCT205, 74VCT206, 54VCT206, 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74VCT257, 54VCT257, 74VCT258, 54VCT258, 74VCT259, 54VCT259, 74VCT260, 54VCT260, 74VCT261, 54VCT261, 74VCT262, 54VCT262, 74VCT263, 54VCT263, 74VCT264, 54VCT264, 74VCT265, 54VCT265, 74VCT266, 54VCT266, 74VCT267, 54VCT267, 74VCT268, 54VCT268, 74VCT269, 54VCT269, 74VCT270, 54VCT270, 74VCT271, 54VCT271, 74VCT272, 54VCT272, 74VCT273, 54VCT273, 74VCT274, 54VCT274, 74VCT275, 54VCT275, 74VCT276, 54VCT276, 74VCT277, 54VCT277, 74VCT278, 54VCT278, 74VCT279, 54VCT279, 74VCT280, 54VCT280, 74VCT281, 54VCT281, 74VCT282, 54VCT282, 74VCT283, 54VCT283, 74VCT284, 54VCT284, 74VCT285, 54VCT285, 74VCT286, 54VCT286, 74VCT287, 54VCT287, 74VCT288, 54VCT288, 74VCT289, 54VCT289, 74VCT290, 54VCT290, 74VCT291, 54VCT291, 74VCT292, 54VCT292, 74VCT293, 54VCT293, 74VCT294, 54VCT294, 74VCT295, 54VCT295, 74VCT296, 54VCT296, 74VCT297, 54VCT297, 74VCT298, 54VCT298, 74VCT299, 54VCT299, 74VCT300, 54VCT300, 74VCT301, 54VCT301, 74VCT302, 54VCT302, 74VCT303, 54VCT303, 74VCT304, 54VCT304, 74VCT305, 54VCT305, 74VCT306, 54VCT306, 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74VCT357, 54VCT357, 74VCT358, 54VCT358, 74VCT359, 54VCT359, 74VCT360, 54VCT360, 74VCT361, 54VCT361, 74VCT362, 54VCT362, 74VCT363, 54VCT363, 74VCT364, 54VCT364, 74VCT365, 54VCT365, 74VCT366, 54VCT366, 74VCT367, 54VCT367, 74VCT368, 54VCT368, 74VCT369, 54VCT369, 74VCT370, 54VCT370, 74VCT371, 54VCT371, 74VCT372, 54VCT372, 74VCT373, 54VCT373, 74VCT374, 54VCT374, 74VCT375, 54VCT375, 74VCT376, 54VCT376, 74VCT377, 54VCT377, 74VCT378, 54VCT378, 74VCT379, 54VCT379, 74VCT380, 54VCT380, 74VCT381, 54VCT381, 74VCT382, 54VCT382, 74VCT383, 54VCT383, 74VCT384, 54VCT384, 74VCT385, 54VCT385, 74VCT386, 54VCT386, 74VCT387, 54VCT387, 74VCT388, 54VCT388, 74VCT389, 54VCT389, 74VCT390, 54VCT390, 74VCT391, 54VCT391, 74VCT392, 54VCT392, 74VCT393, 54VCT393, 74VCT394, 54VCT394, 74VCT395, 54VCT395, 74VCT396, 54VCT396, 74VCT397, 54VCT397, 74VCT398, 54VCT398, 74VCT399, 54VCT399, 74VCT400, 54VCT400, 74VCT401, 54VCT401, 74VCT402, 54VCT402, 74VCT403, 54VCT403, 74VCT404, 54VCT404, 74VCT405, 54VCT405, 74VCT406, 54VCT406, 74VCT407, 54VCT407, 74VCT408, 54VCT408, 74VCT409, 54VCT409, 74VCT410, 54VCT410, 74VCT411, 54VCT411, 74VCT412, 54VCT412, 74VCT413, 54VCT413, 74VCT414, 54VCT414, 74VCT415, 54VCT415, 74VCT416, 54VCT416, 74VCT417, 54VCT417, 74VCT418, 54VCT418, 74VCT419, 54VCT419, 74VCT420, 54VCT420, 74VCT421, 54VCT421, 74VCT422, 54VCT422, 74VCT423, 54VCT423, 74VCT424, 54VCT424, 74VCT425, 54VCT425, 74VCT426, 54VCT426, 74VCT427, 54VCT427, 74VCT428, 54VCT428, 74VCT429, 54VCT429, 74VCT430, 54VCT430, 74VCT431, 54VCT431, 74VCT432, 54VCT432, 74VCT433, 54VCT433, 74VCT434, 54VCT434, 74VCT435, 54VCT435, 74VCT436, 54VCT436, 74VCT437, 54VCT437, 74VCT438, 54VCT438, 74VCT439, 54VCT439, 74VCT440, 54VCT440, 74VCT441, 54VCT441, 74VCT442, 54VCT442, 74VCT443, 54VCT443, 74VCT444, 54VCT444, 74VCT445, 54VCT445, 74VCT446, 54VCT446, 74VCT447, 54VCT447, 74VCT448, 54VCT448, 74VCT449, 54VCT449, 74VCT450, 54VCT450, 74VCT451, 54VCT451, 74VCT452, 54VCT452, 74VCT453, 54VCT453, 74VCT454, 54VCT454, 74VCT455, 54VCT455, 74VCT456, 54VCT456, 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74VCT507, 54VCT507, 74VCT508, 54VCT508, 74VCT509, 54VCT509, 74VCT510, 54VCT510, 74VCT511, 54VCT511, 74VCT512, 54VCT512, 74VCT513, 54VCT513, 74VCT514, 54VCT514, 74VCT515, 54VCT515, 74VCT516, 54VCT516, 74VCT517, 54VCT517, 74VCT518, 54VCT518, 74VCT519, 54VCT519, 74VCT520, 54VCT520, 74VCT521, 54VCT521, 74VCT522, 54VCT522, 74VCT523, 54VCT523, 74VCT524, 54VCT524, 74VCT525, 54VCT525, 74VCT526, 54VCT526, 74VCT527, 54VCT527, 74VCT528, 54VCT528, 74VCT529, 54VCT529, 74VCT530, 54VCT530, 74VCT531, 54VCT531, 74VCT532, 54VCT532, 74VCT533, 54VCT533, 74VCT534, 54VCT534, 74VCT535, 54VCT535, 74VCT536, 54VCT536, 74VCT537, 54VCT537, 74VCT538, 54VCT538, 74VCT539, 54VCT539, 74VCT540, 54VCT540, 74VCT541, 54VCT541, 74VCT542, 54VCT542, 7



# CD54/74AC564, CD54/74AC574 CD54/74ACT564, CD54/74ACT574

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS				V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
						+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	V <sub>IH</sub>	—	4.5 to 5.5	2	—	2	—	2	—	V		
Low-Level Input Voltage	V <sub>IL</sub>	—	4.5 to 5.5	0.8	—	0.8	—	0.8	—	V		
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	—	4.4	—	4.4	—	V	
		#	-24	4.5	3.94	—	3.8	—	3.7	—		
		*	-75	5.5	—	—	3.85	—	—	—		
		*	-50	5.5	—	—	—	—	3.85	—		
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	—	0.1	—	0.1	—	0.1	V	
		#	24	4.5	—	0.36	—	0.44	—	0.5		
		*	75	5.5	—	—	1.65	—	—	—		
		*	50	5.5	—	—	—	—	—	1.65		
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA		
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>	—	—	—	—	—	—	—	—	μA	
		V <sub>O</sub> =V <sub>CC</sub> or GND	—	5.5	—	±0.5	—	±5	—	±10		
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA	
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> =2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA		

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
D, OE CP	0.7 1.17

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristic Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC564, CD54/74AC574

## CD54/74ACT564, CD54/74ACT574

## PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width	t <sub>W</sub>	1.5 3.3* 5†	75 11 5.9	— — —	85 12 6.7	— — —	ns
Setup Time Data to Clock	t <sub>SU</sub>	1.5 3.3 5	2 2 2	— — —	2 2 2	— — —	ns
Hold Time Data to Clock	t <sub>H</sub>	1.5 3.3 5	2 2 2	— — —	2 2 2	— — —	ns
Maximum Clock Frequency	f <sub>MAX</sub>	1.5 3.3 5	6.5 48 85	— — —	6 42 75	— — —	MHz

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

5 V: min is @ 4.75 V for 0 to +70°C

SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
Clock to Q	t <sub>PLH</sub>	1.5	—	140	—	157	ns
AC574	t <sub>PHL</sub>	3.3*	5.3	15.8	3.3	17.6	
		5†	2.3	11.3	2.2	12.6	
Clock to $\overline{Q}$							
AC564	t <sub>PLH</sub>	1.5	—	128	—	140	ns
	t <sub>PHL</sub>	3.3	3.1	14.3	2.9	15.8	
		5	2.1	10.2	1.9	11.3	
Output Enable and Disable to Q							
AC574	t <sub>PLZ</sub>	1.5	—	162	—	181	ns
	t <sub>PHZ</sub>	3.3	4.2	19.5	4.1	21.8	
	t <sub>PZL</sub> t <sub>PZH</sub>	5	2.7	13	2.6	14.5	
Output Enable and Disable to $\overline{Q}$							
AC564	t <sub>PLZ</sub>	1.5	—	162	—	181	ns
	t <sub>PHZ</sub>	3.3	4.2	19.5	4.1	21.8	
	t <sub>PZL</sub> t <sub>PZH</sub>	5	2.7	13	2.6	14.5	
Power Dissipation Capacitance	C <sub>PD</sub> §	—	60 Typ.		60 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V†5 V: min. is @ 5.5 V  
max. is @ 4.5 V5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C§C<sub>PD</sub> is used to determine the dynamic power consumption, per flip flop.

$$P_D = C_{PD} V_{CC}^2 f_i + \sum V_{CC}^2 f_o C_L \text{ where } f_i = \text{input frequency}$$

$$f_o = \text{output frequency}$$

$$C_L = \text{output load capacitance}$$

$$V_{CC} = \text{supply voltage.}$$

# CD54/74AC564, CD54/74AC574 CD54/74ACT564, CD54/74ACT574

## PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width	t <sub>w</sub>	5†	6.7	—	7.4	—	ns
Setup Time Data to Clock	t <sub>SU</sub>	5	2	—	2	—	ns
Hold Time Data to Clock	t <sub>H</sub>	5	2	—	2	—	ns
Maximum Clock Frequency	f <sub>MAX</sub>	5	75	—	68	—	MHz

†5 V: min. is @ 4.5 V

5 V: min. is @ 4.75 V for 0 to +70°C

## SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Clock to Q ACT574	t <sub>PLH</sub> t <sub>PHL</sub>	5†	2.3	11.4	2.2	12.7	ns
Clock to $\bar{Q}$ ACT564	t <sub>PLH</sub> t <sub>PHL</sub>	5	2.1	10.6	2	11.7	ns
Output Enable and Disable to Q ACT574	t <sub>PLZ</sub> t <sub>PHZ</sub> t <sub>PZL</sub> t <sub>PZH</sub>	5	2.7	13	2.6	14.5	ns
Output Enable and Disable to $\bar{Q}$ ACT564	t <sub>PLZ</sub> t <sub>PHZ</sub> t <sub>PZL</sub> t <sub>PZH</sub>	5	2.7	13	2.6	14.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	72 Typ.		72 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per flip flop.

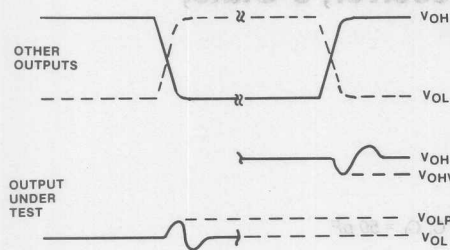
$$P_D = C_{PD} V_{CC}^2 f_i + \sum V_{CC}^2 f_o C_L + V_{CC} \Delta I_{CC} \text{ where } f_i = \text{input frequency}$$

$$f_o = \text{output frequency}$$

$$C_L = \text{output load capacitance}$$

$$V_{CC} = \text{supply voltage.}$$

# PARAMETER MEASUREMENT INFORMATION

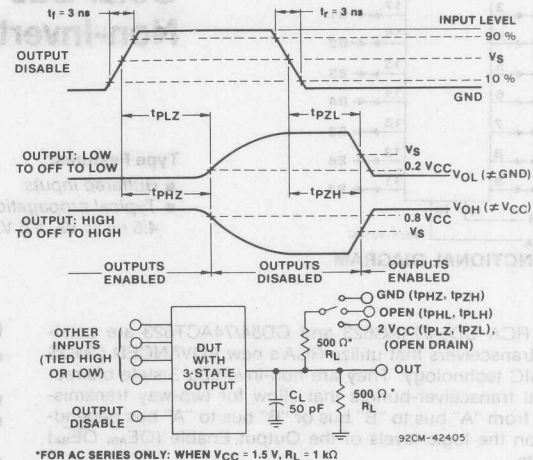


## NOTES:

1.  $V_{OHV}$  and  $V_{OLP}$  ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:  
 $PRR \leq 1 \text{ MHz}$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ , SKEW  $1 \text{ ns}$ .
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.  
 IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH  $0.1 \mu\text{F}$  CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

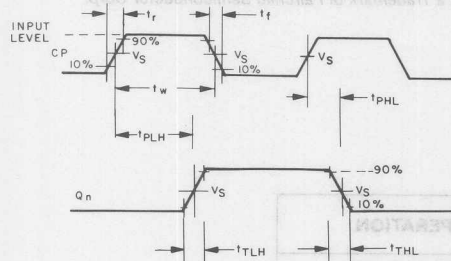
92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.



\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

Fig. 2 - Three-state propagation delay waveforms and test circuit.

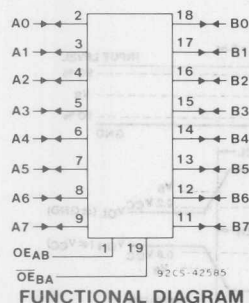


\*FOR AC SERIES ONLY: WHEN  
 $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

92CS-42389

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$

Fig. 3 - Propagation delays times and test circuit.



## Octal-Bus Transceiver, 3-State, Non-Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay:  
4.5 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

The RCA CD54/74AC623 and CD54/74ACT623 are octal-bus transceivers that utilize RCA's new ADVANCED CMOS LOGIC technology. They are non-inverting 3-state bidirectional transceiver-buffers that allow for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus depending on the logic levels of the Output Enable ( $OE_{AB}$ ,  $OE_{BA}$ ) inputs.

The dual Output Enable provision gives these devices the capability to store data by simultaneously enabling  $OE_{AB}$  and  $OE_{BA}$ . Each output reinforces its input under these conditions, and when all other data sources to the bus lines are at high-impedance, both sets of bus lines will remain in their last states.

The CD54AC623 and CD54ACT623 are supplied in 20-lead dual-in-line ceramic packages (F suffix). The CD74AC623 and CD74ACT623 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST<sup>®</sup>/AS/S with significantly reduced power
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST<sup>®</sup> ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

**TRUTH TABLE**

OUTPUT ENABLE INPUTS		OPERATION
$\overline{OE}_{BA}$	$OE_{AB}$	
L	L	B DATA TO A BUS
H	H	A DATA TO B BUS
H	L	ISOLATION
L	H	B DATA TO A BUS, A DATA TO B BUS

H = High level, L = Low level

Note: To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10 k $\Omega$  to 1 M $\Omega$  resistors.

CD54/74ACT623	CD54/74AC623	Input Level
3 V	$V_{CC}$	Input Switching Voltage, V <sub>CC</sub>
5 V	0.5 V <sub>CC</sub>	Input Switching Voltage, V <sub>CC</sub>
0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>	Output Switching Voltage, V <sub>CC</sub>



# CD54/74AC623 CD54/74ACT623

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ OR GROUND CURRENT ( $I_{CC}$ OR $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{STG}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

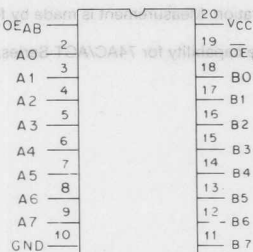
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ †: (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I, V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

†Unless otherwise specified, all voltages are referenced to ground.



TERMINAL ASSIGNMENT

# CD54/74AC623 CD54/74ACT623

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
						+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V <sub>IH</sub>					1.5	1.2	—	1.2	—	1.2	—	V
					3	2.1	—	2.1	—	2.1	—	
					5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V <sub>IL</sub>					1.5	—	0.3	—	0.3	—	0.3	V
					3	—	0.9	—	0.9	—	0.9	
					5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V <sub>OH</sub>			V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
				-0.05	3	2.9	—	2.9	—	2.9	—	
				-0.05	4.5	4.4	—	4.4	—	4.4	—	
				-4	3	2.58	—	2.48	—	2.4	—	
				-24	4.5	3.94	—	3.8	—	3.7	—	
				-75	5.5	—	—	3.85	—	—	—	
				-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V <sub>OL</sub>			V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
				0.05	3	—	0.1	—	0.1	—	0.1	
				0.05	4.5	—	0.1	—	0.1	—	0.1	
				12	3	—	0.36	—	0.44	—	0.5	
				24	4.5	—	0.36	—	0.44	—	0.5	
				75	5.5	—	—	—	1.65	—	—	
				50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I <sub>I</sub>			V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current I <sub>OZ</sub>			V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI I <sub>CC</sub>			V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS		
			+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	$V_{IH}$		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	$V_{IL}$		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		#	-24	4.5	3.94	—	3.8	—	3.7	—	
		*	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		#	24	4.5	—	0.36	—	0.44	—	0.5	
		*	75	5.5	—	—	—	1.65	—	—	
		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	$I_I$	$V_{CC}$ or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	$I_{OZ}$	$V_{IH}$ or $V_{IL}$ $V_O = V_{CC}$ or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	$I_{CC}$	$V_{CC}$ or GND	5.5	—	8	—	80	—	160	μA	
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	$\Delta I_{CC}$	$V_{CC-2.1}$	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum : Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
$A_n, B_n$	0.83
$OE_{BA}$	0.64
$OE_{AB}$	0.15

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# Technical Data

## CD54/74AC623 CD54/74ACT623

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3* 5†	— 2.8 1.8	108 12 8.6	— 2.1 1.7	120 13.4 9.6	ns
Output Disable to Output	t <sub>PLZ</sub> t <sub>PHZ</sub>	1.5 3.3 5	— 3.9 2.5	150 15 12	— 3.8 2.4	167 16.8 13.4	ns
Output Enable to Output	t <sub>PZL</sub> t <sub>PZH</sub>	1.5 3.3 5	— 3.9 2.5	150 18 12	— 3.8 2.4	167 20.1 13.4	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	66 Typ.		66 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output	t <sub>PLH</sub> t <sub>PHL</sub>	5†	1.9	9.6	1.8	10.6	ns
Output Disable to Output	t <sub>PLZ</sub> t <sub>PHZ</sub>	5	2.6	13	2.5	14.4	ns
Output Enable to Output	t <sub>PZH</sub> t <sub>PZL</sub>	5	2.6	13	2.5	14.4	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	79 Typ.		79 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>i</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>o</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§ $C_{PD}$  is used to determine the dynamic power consumption, per channel.

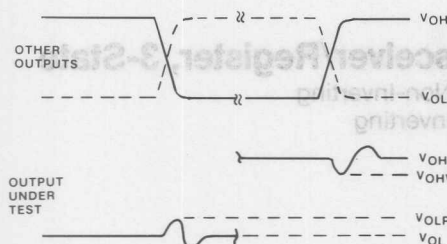
For AC series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

# CD54/74AC623

## CD54/74ACT623

### PARAMETER MEASUREMENT INFORMATION



#### NOTES:

1.  $V_{OHV}$  and  $V_{OLP}$  ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:  
PRR = 1 MHz,  $t_r$  = 3 ns,  $t_f$  = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.  
IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1  $\mu$ F CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

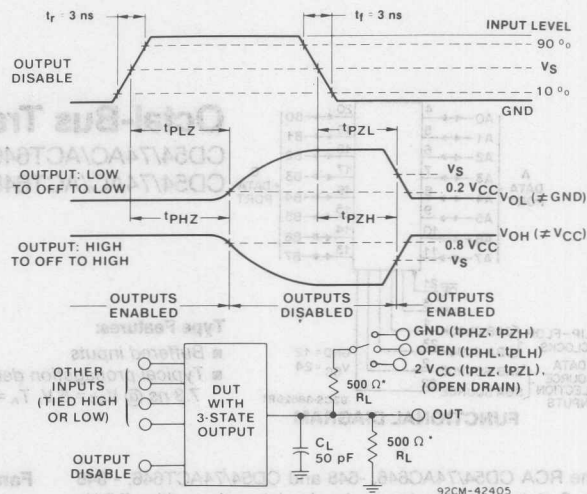


Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Three-state propagation delay times and test circuit.

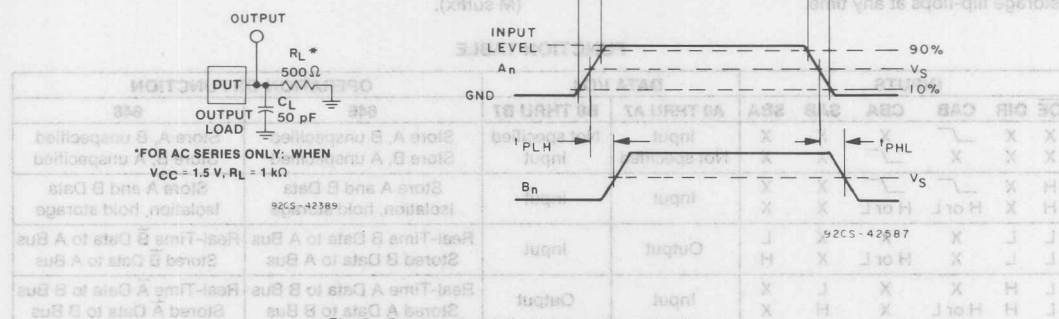


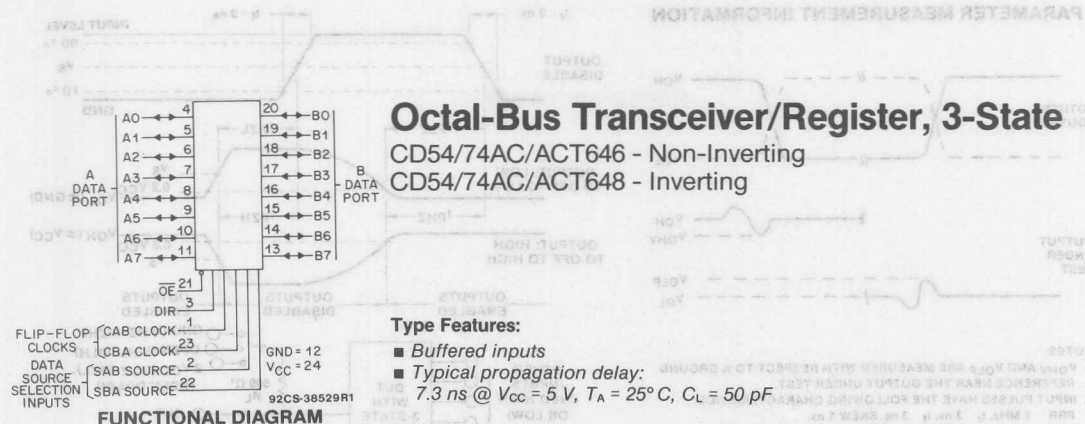
Fig. 3 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$



# CD54/74AC646, CD54/74AC648 CD54/74ACT646, CD54/74ACT648

Product Preview



The RCA CD54/74AC646, -648 and CD54/74ACT646, -648 are 3-state octal-bus transceiver/registers that utilize RCA's new ADVANCED CMOS LOGIC technology. The CD54/74AC648 and CD54/74ACT648 have inverting outputs. The CD54/74AC646 and CD54/74ACT646 have non-inverting outputs. These devices are bus transceivers with D-type flip-flops which act as internal storage registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output Enable ( $\overline{OE}$ ) and Direction (DIR) inputs control the transceiver functions. Data present at the high-impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The Select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The Direction control determines which data bus will receive data when the Output Enable ( $\overline{OE}$ ) is LOW. In the high-impedance mode (Output Enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the Direction (DIR) and Output Enable ( $\overline{OE}$ ) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

## Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24$ -mA output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

The CD54AC/ACT646 and CD54AC/ACT648 are supplied in 24-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT646 and CD74AC/ACT648 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix).

FUNCTION TABLE

INPUTS						DATA I/O#		OPERATION OR FUNCTION	
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	646	648
X	X	X	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	X	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	X	X	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B Data to A Bus	Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time A Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus	Stored A Data to B Bus

#The data output functions may be enabled or disabled by various signals at the  $\overline{OE}$  and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

To prevent excess currents in the High-Z modes, all I/O terminals should be terminated with 10 k $\Omega$  resistors.

Output Switching Voltage, $V_{OS}$	Input Switching Voltage, $V_{IS}$	Input Level, $V_{IL}$
0.5 V	0.5 V	0.5 V
0.5 V	0.5 V	0.5 V
0.5 V	0.5 V	0.5 V

File Number 1970

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

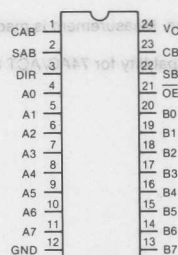
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ * (For $T_A =$ Full Package-Temperature Range)			V
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			$^\circ\text{C}$
CD74 Types	-40	+125	$^\circ\text{C}$
CD54 Types	-55	+125	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			ns/V
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.



92CS-36847R1

**TERMINAL ASSIGNMENT**

# CD54/74AC646, CD54/74AC648

## CD54/74ACT646, CD54/74ACT648

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
						+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)				MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V <sub>IH</sub>					1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V
Low-Level Input Voltage V <sub>IL</sub>					1.5 3 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V
High-Level Output Voltage V <sub>OH</sub>			V <sub>IH</sub> or V <sub>IL</sub>  # *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
				-0.05	3	2.9	—	2.9	—	2.9	—	
				-0.05	4.5	4.4	—	4.4	—	4.4	—	
				-4	3	2.58	—	2.48	—	2.4	—	
				-24	4.5	3.94	—	3.8	—	3.7	—	
				-75 -50	5.5 5.5	— —	— —	3.85 —	— —	— 3.85	— —	
Low-Level Output Voltage V <sub>OL</sub>			V <sub>IH</sub> or V <sub>IL</sub>  # *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
				0.05	3	—	0.1	—	0.1	—	0.1	
				0.05	4.5	—	0.1	—	0.1	—	0.1	
				12	3	—	0.36	—	0.44	—	0.5	
				24	4.5	—	0.36	—	0.44	—	0.5	
				75 50	5.5 5.5	— —	— —	— —	1.65 —	— —	— 1.65	
Input Leakage Current I <sub>I</sub>			V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I <sub>OZ</sub>			V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I <sub>CC</sub>			V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

# CD54/74AC646, CD54/74AC648 CD54/74ACT646, CD54/74ACT648

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS		
			+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	V <sub>IH</sub>	4.5 to 5.5	2	—	2	—	2	—	V		
Low-Level Input Voltage	V <sub>IL</sub>	4.5 to 5.5	—	0.8	—	0.8	—	0.8	V		
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	—	4.4	—	4.4	—	
		#	-24	4.5	3.94	—	3.8	—	3.7	—	
		*	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	—	0.1	—	0.1	—	0.1	
		#	24	4.5	—	0.36	—	0.44	—	0.5	
		*	75	5.5	—	—	1.65	—	—	—	
		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	—	5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	—	5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> = 2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

## ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
DIR	0.67
OE	1.17
An, Bn	0.4

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# Technical Data

## CD54/74AC646, CD54/74AC648 CD54/74ACT646, CD54/74ACT648

### PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f <sub>max</sub>	1.5 3.3* 5†	—	—	—	—	MHz
Setup Time Data to Clock	t <sub>su</sub>	1.5 3.3 5	—	—	—	—	ns
Hold Time Data to Clock	t <sub>h</sub>	1.5 3.3 5	—	—	—	—	ns
Clock Pulse Width	t <sub>w</sub>	1.5 3.3 5	—	—	—	—	ns

### SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Store A Data to B Bus Store B Data to A Bus	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3* 5†	— 4.2 2.8	174 19.5 13.9	— 4 2.7	194 21.7 15.5	ns
Store A Data to B Bus Store B Data to A Bus	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 4.2 2.8	174 19.5 13.9	— 4 2.7	194 21.7 15.5	ns
A Data to B Bus B Data to A Bus	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 3.8 2.6	159 17.8 12.7	— 3.7 2.4	178 19.9 14.2	ns
A Data to B Bus B Data to A Bus	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 3.8 2.6	159 17.8 12.7	— 3.7 2.4	178 19.9 14.2	ns
Select to Data	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 4.2 2.8	174 19.5 13.9	— 4 2.7	194 21.7 15.5	ns
Select to Data	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 4.2 2.8	174 19.5 13.9	— 4 2.7	194 21.7 15.5	ns
3-State Enabling/Disabling Time Bus to Output or Register to Output	t <sub>PZH</sub> t <sub>PLZ</sub> t <sub>PHZ</sub>	1.5 3.3 5	— 4.2 2.8	174 20.9 13.9	— 4 2.7	194 23.3 15.5	ns
Power Dissipation Capacitance	C <sub>PD</sub>	—	—	—	—	—	pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Input Capacitance	C <sub>i</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>o</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per package.

P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> C<sub>PD</sub> f<sub>i</sub> + Σ (V<sub>CC</sub><sup>2</sup> C<sub>L</sub> f<sub>o</sub>) where f<sub>i</sub> = input frequency  
f<sub>o</sub> = output frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.



# PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f <sub>max</sub>	5*		—		—	MHz
Setup Time Data to Clock	t <sub>su</sub>	5		—		—	ns
Hold Time Data to Clock	t <sub>h</sub>	5		—		—	ns
Clock Pulse Width	t <sub>w</sub>	5		—		—	ns

\*min. is @ 4.5 V  
min. is @ 4.75 V for 0 to +70°C

## SWITCHING CHARACTERISTICS: ACT Series; t<sub>i</sub> = 3 ns, C<sub>L</sub> = 50 pF

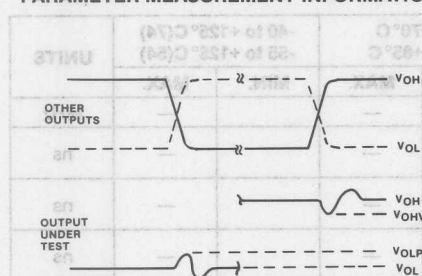
CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Store A Data to B Bus Store B Data to A Bus 646	t <sub>PLH</sub> t <sub>PHL</sub>	5*	2.8	13.9	2.7	15.5	ns
Store A Data to B Bus Store B Data to A Bus 648	t <sub>PLH</sub> t <sub>PHL</sub>	5	2.8	13.9	2.7	15.5	ns
A Data to B Bus B Data to A Bus 646	t <sub>PLH</sub> t <sub>PHL</sub>	5	2.6	12.7	2.4	14.2	ns
A Data to B Bus B Data to A Bus 648	t <sub>PLH</sub> t <sub>PHL</sub>	5	2.6	12.7	2.4	14.2	ns
Select to Data 646	t <sub>PLH</sub> t <sub>PHL</sub>	5	2.8	13.9	2.7	15.5	ns
Select to Data 648	t <sub>PLH</sub> t <sub>PHL</sub>	5	2.8	13.9	2.7	15.5	ns
3-State Enabling/Disabling Time Bus to Output or Register to Output	t <sub>PZL</sub> t <sub>PZH</sub> t <sub>PLZ</sub> t <sub>PHZ</sub>	5	2.8	13.9	2.7	15.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—					pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>i</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

\*min. is @ 5.5 V  
max. is @ 4.5 V  
min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

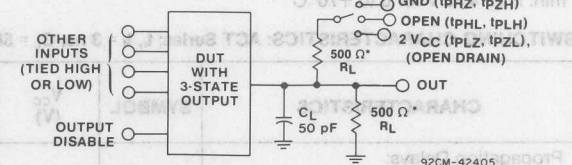
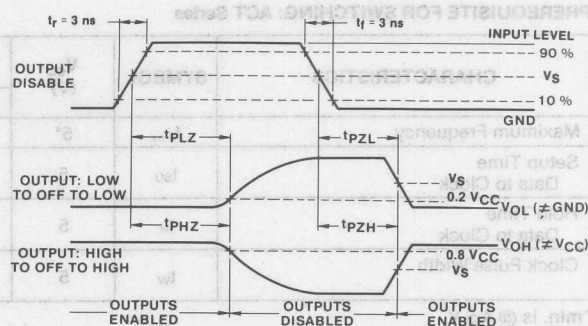
§C<sub>PD</sub> is used to determine the dynamic power consumption, per package.  
P<sub>D</sub> = C<sub>PD</sub>V<sub>CC</sub><sup>2</sup>f<sub>i</sub> + Σ (C<sub>L</sub>V<sub>CC</sub><sup>2</sup>f<sub>o</sub>) + V<sub>CC</sub>ΔI<sub>CC</sub> where f<sub>i</sub> = input frequency  
f<sub>o</sub> = output frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.

**CD54/74AC646, CD54/74AC648**  
**CD54/74ACT646, CD54/74ACT648**

### PARAMETER MEASUREMENT INFORMATION



- NOTES:
1.  $V_{OH}$  AND  $V_{OL}$  ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
  2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR = 1 MHz,  $t_r = 3$  ns,  $t_f = 3$  ns, SKEW 1 ns.
  3. R.F. FIXTURE WITH 700-MHZ DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1  $\mu$ F CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.



\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Three-state propagation delay waveforms and test circuit.

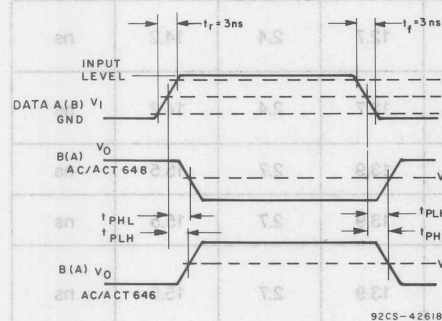


Fig. 3 - Propagation delay times.

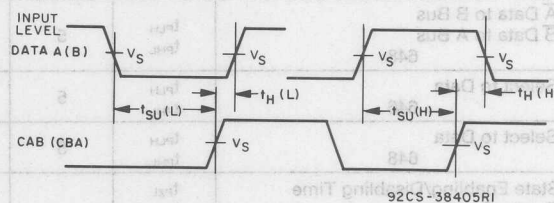
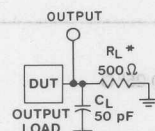


Fig. 4 - Data setup and hold times.



\*FOR AC SERIES ONLY: WHEN  
 $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

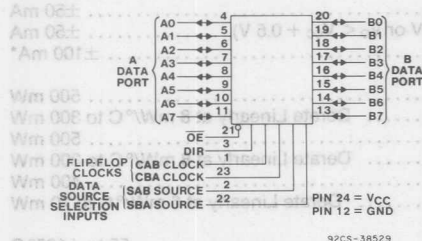
	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_s$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_s$	0.5 $V_{CC}$	0.5 $V_{CC}$

*Fig. 5 - Test circuit.*

## Product Preview

# CD54/74AC647, CD54/74AC649

## CD54/74ACT647, CD54/74ACT649



FUNCTIONAL DIAGRAM

The RCA CD54/74AC647, -649 and CD54/74ACT647, -649 are open-drain, octal-bus transceiver/registers that utilize RCA's new ADVANCED CMOS LOGIC technology. The CD54/74AC649 and CD54/74ACT649 have inverting outputs. The CD54/74AC647 and CD54/74ACT647 have non-inverting outputs. These devices are bus transceivers with D-type flip-flops which act as internal storage registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output Enable ( $\overline{OE}$ ) and Direction (DIR) inputs control the transceiver functions. Data present at the high-impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The Select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The Direction control determines which data bus will receive data when the Output Enable ( $\overline{OE}$ ) is LOW. In the high-impedance mode (Output Enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the Direction (DIR) and Output Enable ( $\overline{OE}$ ) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

### Octal-Bus Transceiver/Register, with Open Drain

CD54/74AC/ACT647 - Non-Inverting  
CD54/74AC/ACT649 - Inverting

## Type Features:

- Buffered inputs
- Typical propagation delay:  
7 ns @  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50 pF$

## Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24$ -mA output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

The CD54AC/ACT647 and CD54AC/ACT649 are supplied in 24-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT647 and CD74AC/ACT649 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix).

FUNCTION TABLE

INPUTS						DATA I/O#		OPERATION OR FUNCTION	
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	AD THRU A7	B0 THRU B7	647	649
X	X		X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X		X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X			X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Store $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

#The data output functions may be enabled or disabled by various signals at the  $\overline{OE}$  and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

To prevent excess currents in the High-Z modes, all I/O terminals should be terminated with 10 k $\Omega$  resistors.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	.....	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	.....	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	.....	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	.....	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	.....	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):		
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	.....	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	.....	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	.....	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	.....	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	.....	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	.....	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):		
PACKAGE TYPE F	.....	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	.....	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{STG}$ )	.....	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	.....	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	.....	$+300^\circ\text{C}$

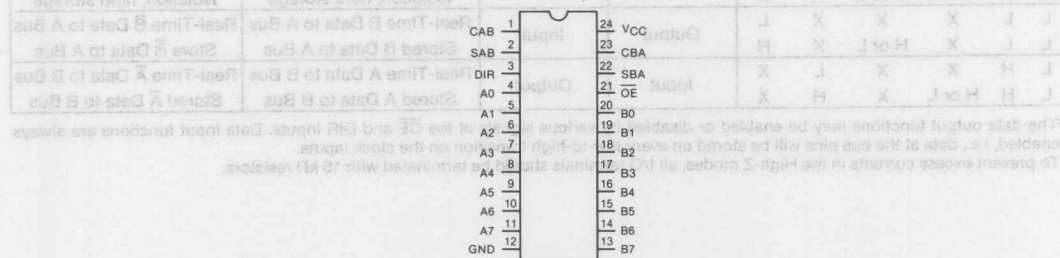
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A$ = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I$ , $V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	-40	$+125$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.



92CS-36847R1

**TERMINAL ASSIGNMENT**

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS					V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)				
	MIN.	MAX.	MIN.	MAX.			MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	—	2	V <sub>IH</sub>	—	—	1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V
Low-Level Input Voltage	—	—	V <sub>IL</sub>	—	—	1.5 3 5.5	— 0.3 0.9 1.65	— 0.3 0.9 —	— — 0.9 1.65	— — — —	— — 0.9 1.65	— — 0.9 1.65	V
Low-Level Output Voltage	—	—	V <sub>OL</sub>	—	0.05	1.5	—	0.1	—	0.1	—	0.1	V
	—	—		—	0.05	3	—	0.1	—	0.1	—	0.1	
	—	—		or	0.05	4.5	—	0.1	—	0.1	—	0.1	
	—	—		V <sub>IL</sub>	—12	3	—	0.36	—	0.44	—	0.5	
	—	—		—	24	4.5	—	0.36	—	0.44	—	0.5	
	—	—		#	75	5.5	—	—	—	1.65	—	—	
	—	—		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	—	—	I <sub>I</sub>	V <sub>CC</sub> or GND	—	5.5	—	±0.1	—	±1	—	±1	μA
Off-State Leakage Current	—	—	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>CC</sub> or GND	—	5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	—	—	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

UNIT LOAD*	INPUT
1.28	CAB, CBA
1.2	SAB, SBA
0.87	DII
1.17	OE
0.4	An, Bn

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.



# CD54/74AC647, CD54/74AC649 CD54/74ACT647, CD54/74ACT649

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS				V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
						+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
						MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage		V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage		V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
Low-Level Output Voltage		V <sub>OL</sub>	V <sub>OL</sub> or V <sub>IL</sub>	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5		
			75	5.5	—	—	—	1.65	—	—		
			50	5.5	—	—	—	—	—	1.65		
Input Leakage Current		I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
Off-State Leakage Current		I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI		I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load		ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
DIR	0.67
OE	1.17
An, Bn	0.4

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC647, CD54/74AC649

## CD54/74ACT647, CD54/74ACT649

## PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f <sub>max</sub>	1.5 3.3* 5†	—	—	—	—	MHz
Setup Time Data to Clock	t <sub>su</sub>	1.5 3.3 5	—	—	—	—	ns
Hold Time Data to Clock	t <sub>h</sub>	1.5 3.3 5	—	—	—	—	ns
Clock Pulse Width	t <sub>w</sub>	1.5 3.3 5	—	—	—	—	ns

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

5 V: min. is @ 4.75 V for 0 to +70°C

SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
Stored A Data to B Bus 647	t <sub>PZL</sub>	1.5 3.3* 5†	— 4.2 2.8	174 20.9 13.9	— 4 2.7	194 23.3 15.5	ns
Stored B Data to A Bus 649	t <sub>PLZ</sub>	1.5 3.3 5	— 5.2 3.4	212 21.1 16.9	— 4.7 3.2	232 23.1 18.5	ns
A Data to B Bus 647	t <sub>PZL</sub>	1.5 3.3 5	— 3.8 2.6	159 19.1 12.7	— 3.7 2.4	178 23 14.2	ns
B Data to A Bus 649	t <sub>PLZ</sub>	1.5 3.3 5	— 4.7 3.2	197 19.6 15.7	— 4.4 3	215 21.5 17.2	ns
Select to Data 647, 649	t <sub>PZL</sub>	1.5 3.3 5	— 4.2 2.8	174 20.9 13.9	— 4 2.7	194 23.3 15.5	ns
	t <sub>PLZ</sub>	1.5 3.3 5	— 5.2 3.4	212 21.1 16.9	— 4.7 3.2	232 23.1 18.5	ns
Enable, Disable Times Bus to Output or Register to Output	t <sub>PZL</sub> t <sub>PLZ</sub>	1.5 3.3 5	— 4.2 2.8	174 20.9 13.9	— 4 2.7	194 23.3 15.5	ns
Power Dissipation Capacitance	C <sub>PD</sub>	—	—	—	—	—	pF
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>i</sub>	—	—	10	—	10	pF
Off-State Output Capacitance	C <sub>o</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V†5 V: min. is @ 5.5 V  
max. is @ 4.5 V5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C§C<sub>PD</sub> is used to determine the dynamic power consumption, per package.  
P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> C<sub>PD</sub> f<sub>i</sub> + Σ V<sub>CC</sub><sup>2</sup> C<sub>L</sub> f<sub>o</sub> where f<sub>i</sub> = input frequencyf<sub>o</sub> = output frequencyC<sub>L</sub> = output load capacitanceV<sub>CC</sub> = supply voltage.

# Technical Data

## CD54/74AC647, CD54/74AC649 CD54/74ACT647, CD54/74ACT649

### PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f <sub>max</sub>	5*	—	—	—	—	MHz
Setup Time Data to Clock	t <sub>su</sub>	5	—	—	—	—	ns
Hold Time Data to Clock	t <sub>h</sub>	5	—	—	—	—	ns
Clock Pulse Width	t <sub>w</sub>	5	—	—	—	—	ns

\*5 V: min. is @ 4.5 V  
5 V: min. is @ 4.75 V for 0 to +70°C

### SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
Stored A Data to B Bus	t <sub>PZL</sub>	5*	2.8	13.9	2.7	15.5	ns
Stored B Data to A Bus	t <sub>PLZ</sub>	5	3.4	16.9	3.2	18.5	ns
Stored A Data to B Bus	t <sub>PZL</sub>	5	2.6	12.7	2.4	14.2	ns
Stored B Data to A Bus	t <sub>PLZ</sub>	5	3.2	15.7	3	17.2	ns
Select to Data	t <sub>PZL</sub>	5	2.8	13.9	2.7	15.5	ns
	t <sub>PLZ</sub>	5	3.4	16.9	3.2	18.5	ns
Enable, Disable Times							
Bus to Output or Register to Output	t <sub>PZL</sub> t <sub>PLZ</sub>	5	2.8	13.9	2.7	15.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	—	—	—	—	pF
Max. (Peak) Vol. During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	—	1 Typ. @ 25°C	—	—	V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
Off-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

\*Min. is @ 5.5 V  
max. is @ 4.5 V  
min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per package.

P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> C<sub>PD</sub> f<sub>i</sub> + Σ V<sub>CC</sub><sup>2</sup> C<sub>L</sub> f<sub>o</sub> + V<sub>CC</sub> ΔI<sub>CC</sub> where f<sub>i</sub> = input frequency

f<sub>o</sub> = output frequency

C<sub>L</sub> = output load capacitance

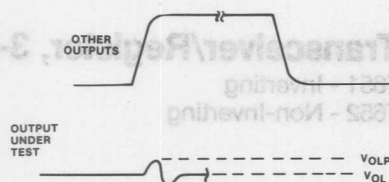
V<sub>CC</sub> = supply voltage.

V	1 Typ. @ 25°C	5	—	—	—	—	—
pF	10	10	—	—	—	—	—
pF	10	15	—	—	—	—	—

§C<sub>PD</sub> is used to determine the dynamic power consumption, per package.  
P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> C<sub>PD</sub> f<sub>i</sub> + Σ V<sub>CC</sub><sup>2</sup> C<sub>L</sub> f<sub>o</sub> + V<sub>CC</sub> ΔI<sub>CC</sub> where f<sub>i</sub> = input frequency  
f<sub>o</sub> = output frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.

\*5.5 V: min. is @ 5.5 V  
max. is @ 4.5 V  
5.25 V: min. is @ 5.25 V  
max. is @ 4.75 V  
5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

## PARAMETER MEASUREMENT INFORMATION



### NOTES:

1. V<sub>OLP</sub> IS MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:  
PRR ≤ 1 MHz, t<sub>r</sub> = 3 ns, t<sub>f</sub> = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.  
IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

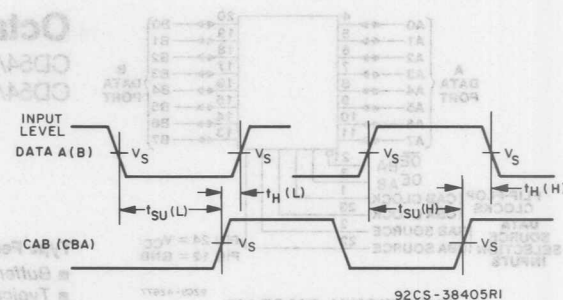


Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Data setup and hold times.

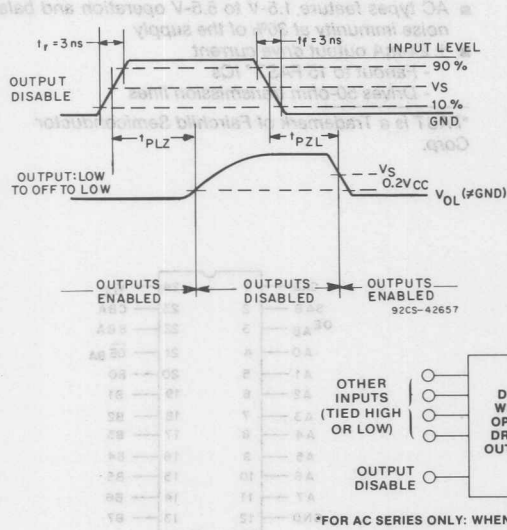
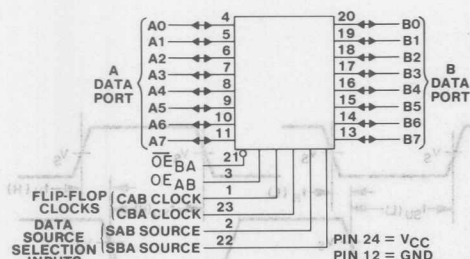


Fig. 3 - Open-drain propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V <sub>CC</sub>	3 V
Input Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	1.5 V
Output Switching Voltage, V <sub>S</sub>	0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>

# CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652

Product Preview



FUNCTIONAL DIAGRAM

## Octal-Bus Transceiver/Register, 3-State

CD54/74AC/ACT651 - Inverting  
CD54/74AC/ACT652 - Non-Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay:  
7.3 ns @  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50pF$

### Family Features:

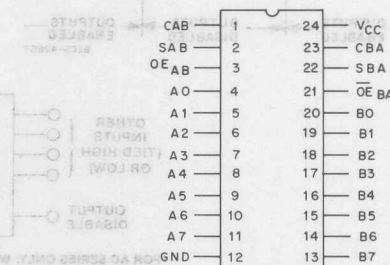
- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24$ -mA output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

The RCA CD54/74AC651, -652 and CD54/74ACT651, -652 are 3-state-octal-bus transceiver/registers that utilize RCA's new ADVANCED CMOS LOGIC technology. The CD54/74AC651 and CD54/74ACT651 have inverting outputs. The CD54/74AC652 and CD54/74ACT652 have non-inverting outputs. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables  $OE_{AB}$  and  $OE_{BA}$  are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer when the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal-bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling  $OE_{AB}$  and  $OE_{BA}$ . In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The CD54AC/ACT651 and CD54AC/ACT652 are supplied in 24-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT651 and CD74AC/ACT652 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix).



TERMINAL ASSIGNMENT

Input Level	Input Switching Voltage, $V_i$	Output Switching Voltage, $V_o$
3.0	3.0	3.0
3.0	3.0	3.0
3.0	3.0	3.0



# CD54/74AC651, CD54/74AC652

## CD54/74ACT651, CD54/74ACT652

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
OE <sub>AB</sub>	OE <sub>BA</sub>	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	651	652
L	H	H or L	H or L	X	X	Input	Input	Isolation*	Isolation*
L	H			X	X	Input	Input	Store A and B Data	Store A and B Data
X	H		H or L	X	X	Input	Unspecified†	Store A, Hold B	Store A, Hold B
H	H			X‡	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L		X	X	Unspecified†	Input	Hold A, Store B	Hold, A Store B
L	L			X	X‡	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A bus	Stored A Data to B Bus Stored B Data to A Bus

\* To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

† The data output functions may be enabled or disabled by various signals at the OE<sub>AB</sub> or OE<sub>BA</sub> inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.

Select control = H: clocks must be staggered in order to load both registers.

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V <sub>CC</sub> )	-0.5 to 6 V
DC INPUT DIODE CURRENT, I <sub>IK</sub> (for V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I <sub>OK</sub> (for V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V)	±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I <sub>O</sub> (for V <sub>O</sub> > -0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V)	±50 mA
DC V <sub>CC</sub> or GROUND CURRENT (I <sub>CC</sub> or I <sub>GND</sub> )	±100 mA*

### POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):

For T <sub>A</sub> = -55 to +100°C (PACKAGE TYPE F)	500 mW
For T <sub>A</sub> = +100 to +125°C (PACKAGE TYPE F)	Derate Linearly at 8 mW/°C to 300 mW
For T <sub>A</sub> = -40 to +100°C (PACKAGE TYPE E)	500 mW
For T <sub>A</sub> = +100 to +125°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T <sub>A</sub> = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T <sub>A</sub> = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW

### OPERATING-TEMPERATURE RANGE (T<sub>A</sub>):

PACKAGE TYPE F	-55 to +125°C
PACKAGE TYPE E, M	-40 to +125°C

### STORAGE TEMPERATURE (T<sub>stg</sub>)

	-65 to +150°C
--	---------------

### LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C
---	--------

Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only	+300°C
---	--------

\*(For up to 4 outputs per device; add ± 25 mA for each additional output.)

### RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V <sub>CC</sub> *: (For T <sub>A</sub> = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V <sub>I</sub> , V <sub>O</sub>	0	V <sub>CC</sub>	V
Operating Temperature, T <sub>A</sub> :			
CD74 Types	-40	+125	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

# STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V
Low-Level Input Voltage	V <sub>IL</sub>			1.5 3 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V
High-Level Output Voltage	V <sub>OH</sub>		-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		V <sub>IH</sub> or V <sub>IL</sub>	-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
		#	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>			0.05	1.5	—	0.1	—	0.1	—	V
		V <sub>IH</sub> or V <sub>IL</sub>		0.05	3	—	0.1	—	0.1	—	
				0.05	4.5	—	0.1	—	0.1	—	
				12	3	—	0.36	—	0.44	—	
				24	4.5	—	0.36	—	0.44	—	
		#		75	5.5	—	—	—	1.65	—	
		*		50	5.5	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> =V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

V	2.5	1.5	AC Types
V	2.5	4.5	ACT Types
V	$V_{CC}$	0	DC Input or Output Voltage, $V_I$ or $V_O$
°C	+125	-40	CDMA Types
°C	+125	-55	CD54 Types
$V_{IH}$	50	0	Input Rise and Fall Rate, dV/dt
$V_{IH}$	50	0	at 1.5 V to 3 V (AC Types)
$V_{IH}$	50	0	at 3.5 V to 5.5 V (AC Types)
$V_{IH}$	10	0	at 1.5 V to 5.5 V (ACT Types)

\*Unless otherwise specified, all voltages are referenced to ground.

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		#	-24	4.5	3.94	—	3.8	—	3.7	—	
		*	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		#	24	4.5	—	0.36	—	0.44	—	0.5	
		*	75	5.5	—	—	—	1.65	—	—	
		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>									μA
		V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> =2.1	—	4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
OE <sub>AB</sub>	0.67
OE <sub>BA</sub>	1.17
An, Bn	0.4

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652

## PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f <sub>max</sub>	1.5 3.3* 5†	—	—	—	—	MHz
Setup Time Data to Clock	t <sub>su</sub>	1.5 3.3 5	—	—	—	—	ns
Hold Time Data to Clock	t <sub>h</sub>	1.5 3.3 5	—	—	—	—	ns
Clock Pulse Data to Clock	t <sub>w</sub>	1.5 3.3 5	—	—	—	—	ns

## SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Store A Data to B Bus Store B Data to A Bus 646	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3* 5†	— 4.2 2.8	174 19.5 13.9	— 4 2.7	194 21.7 15.5	ns
Store A Data to B Bus Store B Data to A Bus 648	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 4.2 2.8	174 19.5 13.9	— 4 2.7	194 21.7 15.5	ns
A Data to B Bus B Data to A Bus 646	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 3.8 2.6	159 17.8 12.7	— 3.7 2.4	178 19.9 14.2	ns
A Data to B Bus B Data to A Bus 648	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 3.8 2.6	159 17.8 12.7	— 3.7 2.4	178 19.9 14.2	ns
Select to Data 646	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 4.2 2.8	174 19.5 13.9	— 4 2.7	194 21.7 15.5	ns
Select to Data 648	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	— 4.2 2.8	174 19.5 13.9	— 4 2.7	194 21.7 15.5	ns
3-State Enabling/ Disabling Time Bus to Output or Register to Output	t <sub>PZL</sub> t <sub>PZH</sub> t <sub>PLZ</sub> t <sub>PHZ</sub>	1.5 3.3 5	— 4.2 2.8	174 20.9 13.9	— 4 2.7	194 23.3 15.5	ns
Power Dissipation Capacitance	C <sub>PD</sub>	—					pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Input Capacitance	C <sub>i</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>o</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per package.

P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> C<sub>PD</sub> f<sub>i</sub> + Σ (V<sub>CC</sub><sup>2</sup> C<sub>L</sub> f<sub>o</sub>) where f<sub>i</sub> = input frequency

f<sub>o</sub> = output frequency

C<sub>L</sub> = output load capacitance

V<sub>CC</sub> = supply voltage.

# CD54/74AC651, CD54/74AC652

## CD54/74ACT651, CD54/74ACT652

## PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	$f_{max}$	5*		—		—	MHz
Setup Time Data to Clock	$t_{su}$	5		—		—	ns
Hold Time Data to Clock	$t_h$	5		—		—	ns
Clock Pulse Width	$t_w$	5		—		—	ns

\*5 V: min. is @ 4.5 V

5 V: min. is @ 4.75 V for 0 to +70°C

SWITCHING CHARACTERISTICS: ACT Series;  $t_i, t_r = 3$  ns,  $C_L = 50$  pF

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Store A Data to B Bus Store B Data to A Bus 646	$t_{PLH}$ $t_{PHL}$	5*	2.8	13.9	2.7	15.5	ns
Store $\bar{A}$ Data to B Bus Store $\bar{B}$ Data to A Bus 646	$t_{PLH}$ $t_{PHL}$	5	2.8	13.9	2.7	15.5	ns
A Data to B Bus B Data to A Bus 646	$t_{PLH}$ $t_{PHL}$	5	2.6	12.7	2.4	14.2	ns
$\bar{A}$ Data to B Bus B Data to A Bus 648	$t_{PLH}$ $t_{PHL}$	5	2.6	12.7	2.4	14.2	ns
Select to Data 646	$t_{PLH}$ $t_{PHL}$	5	2.8	13.9	2.7	15.5	ns
Select to Data 648	$t_{PLH}$ $t_{PHL}$	5	2.8	13.9	2.7	15.5	ns
3-State Enabling/ Disabling Time Bus to Output or Register to Output	$t_{PZH}$ $t_{PLZ}$ $t_{PHZ}$	5	2.8	13.9	2.7	15.5	ns
Power Dissipation Capacitance	$C_{PD}\S$	—					pF
Min. (Valley) During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OH}$  $V_{OHV}$ See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OL}$  $V_{OLP}$ See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	$C_i$	—	—	10	—	10	pF
3-State Output Capacitance	$C_o$	—	—	15	—	15	pF

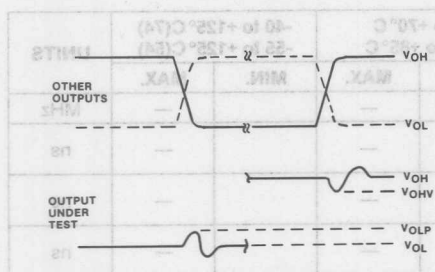
\*5 V: min. is @ 5.5 V  
max. is @ 4.5 V5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C $\S C_{PD}$  is used to determine the dynamic power consumption, per package.
$$P_D = V_{CC}^2 C_{PD} f_i + \sum V_{CC}^2 C_{Lfo} + V_{CC} \Delta I_{CC}$$

where  $f_i$  = input frequency  
 $f_o$  = output frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.



# CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652

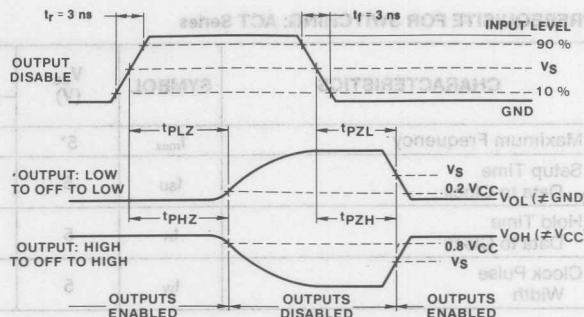
## PARAMETER MEASUREMENT INFORMATION



- NOTES:
1.  $V_{OH}$  and  $V_{OL}$  are measured with respect to a ground reference near the output under test.
  2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:  
 $PRR \leq 1 \text{ MHz}$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ , SKEW 1 ns.
  3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.  
 $IC$  SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH  $0.1 \mu\text{F}$  CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.



\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

Fig. 2 - Three-state propagation delay waveforms and test circuit.

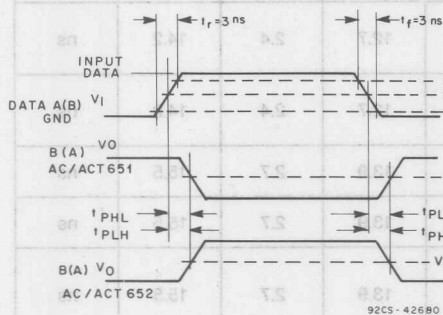


Fig. 3 - Propagation delay times.

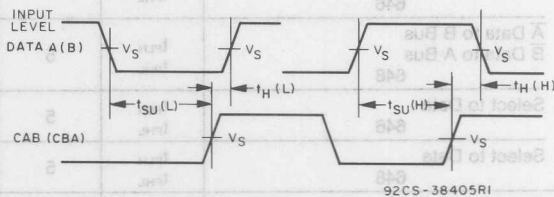
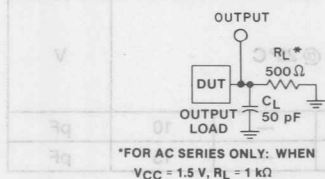


Fig. 4 - Data setup and hold times.

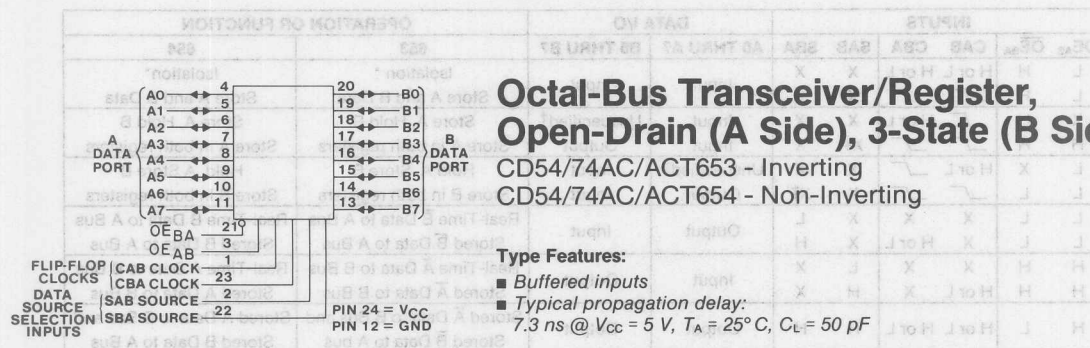


\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

92CS-42589

Fig. 5 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$



## Octal-Bus Transceiver/Register, Open-Drain (A Side), 3-State (B Side)

CD54/74AC/ACT653 - Inverting

CD54/74AC/ACT654 - Non-Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay:  
7.3 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

The RCA CD54/74AC653, -654 and CD54/74ACT653, -654 are octal-bus transceiver/registers that utilize RCA's new ADVANCED CMOS LOGIC technology. The CD54/74AC653 and CD54/74ACT653 are inverting types having open drains on the A outputs and 3-state outputs on the B side. The CD54/74AC654 and CD54/74ACT654 differ only in that these are non-inverting types. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables  $\overline{OE}_{AB}$  and  $\overline{OE}_{BA}$  are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal-bus transceivers and registers.

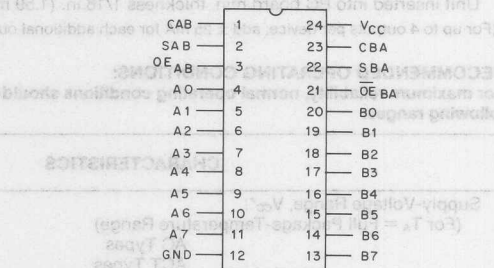
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling  $\overline{OE}_{AB}$  and  $\overline{OE}_{BA}$ . In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The CD54AC/ACT653 and CD54AC/ACT654 are supplied in 24-lead dual-in-line ceramic packages (F suffix). The CD74AC/ACT653 and CD74AC/ACT654 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5 V to 5.5 V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{ mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.



# CD54/74AC653, CD54/74AC654 CD54/74ACT653, CD54/74ACT654

Product Preview

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
OE <sub>AB</sub>	OE <sub>BA</sub>	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	653	654
L	H	H or L	H or L	X	X			Isolation *	Isolation *
L	H			X	X	Input	Input	Store A and B Data	Store A and B Data
X	H		H or L	X	X	Input	Unspecified†	Store A, Hold B	Store A, Hold B
H	H			X‡	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L		X	X	Unspecified†	Input	Hold A, Store B	Hold A, Store B
L	L			X	X‡	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A bus	Stored A Data to B Bus and Stored B Data to A Bus

\* To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

† The data output functions may be enabled or disabled by various signals at the OE<sub>AB</sub> or OE<sub>BA</sub> inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.

Select control = H: clocks should be staggered in order to load both registers.

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V <sub>CC</sub> )	0.5 to 6 V
DC INPUT DIODE CURRENT, I <sub>IK</sub> (for V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I <sub>OK</sub> (for V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V)	±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I <sub>O</sub> (for V <sub>O</sub> > -0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V)	±50 mA
DC V <sub>CC</sub> or GROUND CURRENT (I <sub>CC</sub> or I <sub>GND</sub> )	±100 mA

## POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):

For T <sub>A</sub> = -55 to +100°C (PACKAGE TYPE F)	500 mW
For T <sub>A</sub> = +100 to +125°C (PACKAGE TYPE F)	Derate Linearly at 8 mW/°C to 300 mW
For T <sub>A</sub> = -40 to +100°C (PACKAGE TYPE E)	500 mW
For T <sub>A</sub> = +100 to +125°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T <sub>A</sub> = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T <sub>A</sub> = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW

## OPERATING-TEMPERATURE RANGE (T<sub>A</sub>):

PACKAGE TYPE F	-55 to +125°C
PACKAGE TYPE E, M	-40 to +125°C
STORAGE TEMPERATURE (T <sub>stg</sub> )	-65 to +150°C

## LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only	+300°C

(For up to 4 outputs per device; add ± 25 mA for each additional output.)

## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V <sub>CC</sub> *, (For T <sub>A</sub> = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V <sub>I</sub> , V <sub>O</sub>	0	V <sub>CC</sub>	V
Operating Temperature, T <sub>A</sub> :			
CD74 Types	-40	+125	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\* Unless otherwise specified, all voltages are referenced to ground.

**CD54/74AC653, CD54/74AC654**  
**CD54/74ACT653, CD54/74ACT654**

### STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS			TEST CONDITIONS			AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
						+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
						MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)	V <sub>CC</sub> (V)							
High-Level Input Voltage			V <sub>IH</sub>	—	1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V
Low-Level Input Voltage			V <sub>IL</sub>	—	1.5 3 5.5	— 0.9 1.65	0.3 — 1.65	— 0.9 1.65	0.3 — 1.65	— 0.9 1.65	0.3 — 1.65	V
High-Level Output Voltage (B Side)			V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05 -0.05 -0.05 -4 -24 -75 -50	1.5 3 4.5 3 4.5 5.5 5.5	1.4 2.9 4.4 2.58 3.94 — —	1.4 2.9 4.4 2.48 3.8 3.85 —	— — — — — — —	1.4 2.9 4.4 2.4 3.7 — 3.85	— — — — — — —	V
Low-Level Output Voltage			V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05 0.05 0.05 12 24 75 50	1.5 3 4.5 3 4.5 5.5 5.5	— 0.1 0.1 0.36 0.36 — —	— 0.1 0.1 — 0.44 1.65 —	0.1 0.1 0.1 0.44 0.44 — —	— — — — — — —	0.1 0.1 0.1 0.5 0.5 — 1.65	V
Input Leakage Current			I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA
3-State or Off-State Leakage Current			I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI			I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160 μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.



# Technical Data

## CD54/74AC653, CD54/74AC654 CD54/74ACT653, CD54/74ACT654

### STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS					V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
			V <sub>I</sub> (V)	I <sub>O</sub> (mA)	+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)				
	MIN.	MAX.			MIN.		MAX.	MIN.	MAX.				
High-Level Input Voltage	—	V <sub>IH</sub>	—	—	4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	—	V <sub>IL</sub>	—	—	4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage (B Side)	—	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	—	4.4	—	4.4	—	V	
			V <sub>IH</sub> or V <sub>IL</sub>	-24	4.5	3.94	—	3.8	—	3.7	—		
			#	-75	5.5	—	—	3.85	—	—	—		
			*	-50	5.5	—	—	—	—	3.85	—		
Low-Level Output Voltage	—	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	—	0.1	—	0.1	—	0.1	V	
			V <sub>IH</sub> or V <sub>IL</sub>	24	4.5	—	0.36	—	0.44	—	0.5		
			#	75	5.5	—	—	—	1.65	—	—		
			*	50	5.5	—	—	—	—	—	1.65		
Input Leakage Current	—	I <sub>I</sub>	V <sub>CC</sub> or GND	—	5.5	—	±0.1	—	±1	—	±1	μA	
3-State or Off-State Leakage Current	—	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>	—	5.5	—	±0.5	—	±5	—	±10	μA	
			V <sub>CC</sub> or GND	—	—	—	—	—	—	—	—		
Quiescent Supply Current, MSI	—	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA	
Additional Supply Current per Input Pin, TTL Inputs High 1 Unit Load	—	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	—	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

### ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
OE <sub>AB</sub>	0.67
OE <sub>BA</sub>	1.17
An, Bn	0.4

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.



# PARAMETER MEASUREMENT INFORMATION

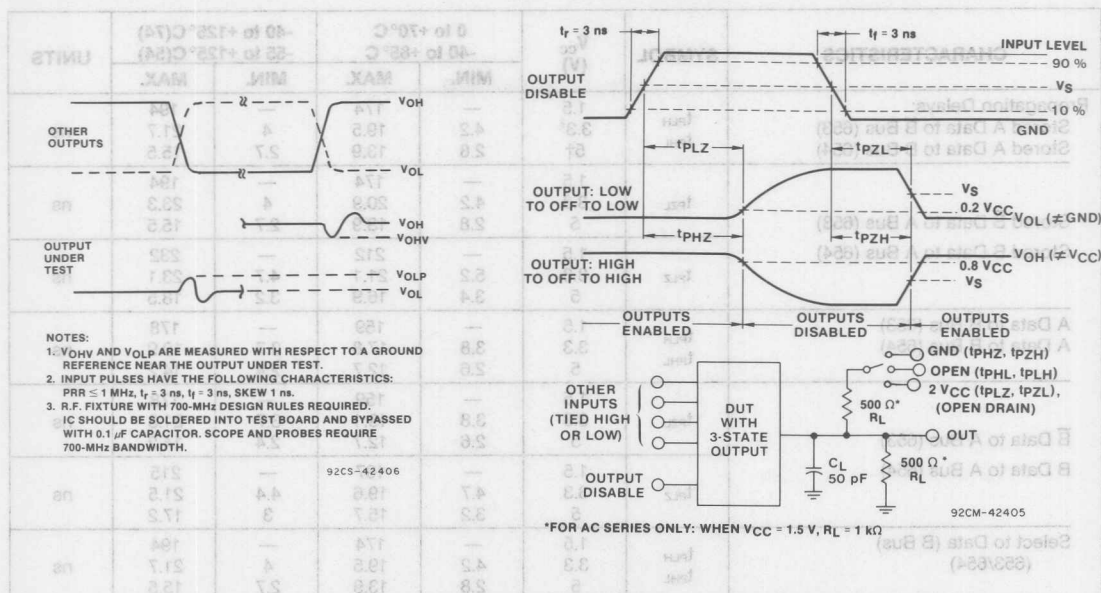


Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Three-state propagation delay waveforms and test circuit (B outputs).

## PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	$f_{max}$	1.5 3.3* 5†	—	—	—	—	MHz
Setup Time Data to Clock	$t_{su}$	1.5 3.3 5	—	—	—	—	ns
Hold Time Data to Clock	$t_h$	1.5 3.3 5	—	—	—	—	ns
Clock Pulse Data to Clock	$t_w$	1.5 3.3 5	—	—	—	—	ns

\* 3.3 V: min. is @ 3 V

† 5 V: min. is @ 4.5 V

5 V: min. is @ 4.75 V for 0 to +70°C

**SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3$  ns,  $C_L = 50$  pF**

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
Stored A Data to $\bar{B}$ Bus (653)	$t_{PLH}$	1.5	—	174	—	194	ns
Stored A Data to B Bus (654)	$t_{PHL}$	3.3*	4.2	19.5	4	21.7	
		5†	2.8	13.9	2.7	15.5	
Stored $\bar{B}$ Data to A Bus (653)	$t_{PZL}$	1.5	—	174	—	194	ns
		3.3	4.2	20.9	4	23.3	
		5	2.8	13.9	2.7	15.5	
Stored B Data to A Bus (654)	$t_{PLZ}$	1.5	—	212	—	232	ns
		3.3	5.2	21.1	4.7	23.1	
		5	3.4	16.9	3.2	18.5	
A Data to $\bar{B}$ Bus (653)	$t_{PLH}$	1.5	—	159	—	178	ns
A Data to B Bus (654)	$t_{PHL}$	3.3	3.8	17.8	3.7	19.9	
		5	2.6	12.7	2.4	14.2	
$\bar{B}$ Data to A Bus (653)	$t_{PZL}$	1.5	—	159	—	178	ns
		3.3	3.8	19.1	3.7	21.3	
		5	2.6	12.7	2.4	14.2	
B Data to A Bus (654)	$t_{PLZ}$	1.5	—	197	—	215	ns
		3.3	4.7	19.6	4.4	21.5	
		5	3.2	15.7	3	17.2	
Select to Data (B Bus) (653/654)	$t_{PLH}$	1.5	—	174	—	194	ns
	$t_{PHL}$	3.3	4.2	19.5	4	21.7	
		5	2.8	13.9	2.7	15.5	
Select to Data (A Bus) (653/654)	$t_{PZL}$	1.5	—	174	—	194	ns
		3.3	4.2	20.9	4	23.3	
		5	2.8	13.9	2.7	15.5	
	$t_{PLZ}$	1.5	—	212	—	232	ns
		3.3	5.2	21.1	4.7	23.1	
		5	3.4	16.9	3.2	18.5	
3-State Enabling/ Disabling Time (B Bus) Bus to Output or Register to Output (653/654)	$t_{PZL}$	1.5	—	174	—	194	ns
	$t_{PZH}$	3.3	4.2	20.9	4	23.3	
	$t_{PLZ}$	5	2.8	13.9	2.7	15.5	
Off-State Enabling/ Disabling Time (A Bus) Bus to Output or Register to Output (653/654)	$t_{PZL}$	1.5	—	174	—	194	ns
	$t_{PLZ}$	3.3	4.2	20.9	4	23.3	
		5	2.8	13.9	2.7	15.5	
Power Dissipation Capacitance	$C_{PD}$	—					pF
Min. (Valley) $V_{OH}$ (B Side) During Switching of Other Outputs (Output Under Test No Switching)	$V_{OHV}$ See Fig. 1	5		4 Typ. @ 25°C			V
Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OLP}$ See Fig. 1	5		1 Typ. @ 25°C			V
Input Capacitance	$C_i$	—	—	10	—	10	pF
3-State Output Capacitance (B Side)	$C_o$	—	—	15	—	15	pF
Off-State Output Capacitance (A Side)	$C_o$	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

$\S C_{PD}$  is used to determine the dynamic power consumption, per package.

$P_D = V_{CC}^2 C_{PD} f_i + \Sigma (V_{CC}^2 C_{L} f_o)$  where  $f_i$  = input frequency  
 $f_o$  = output frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

# CD54/74AC653, CD54/74AC654

## CD54/74ACT653, CD54/74ACT654

## PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f <sub>max</sub>	5*		—		—	MHz
Setup Time Data to Clock	t <sub>su</sub>	5		—		—	ns
Hold Time Data to Clock	t <sub>h</sub>	5		—		—	ns
Clock Pulse Width	t <sub>w</sub>	5		—		—	ns

\*5 V:min. is @ 4.5 V

5 V:min. is @ 4.75 V for 0 to +70°C

SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	0 to +70°C -40 to +85°C		-40 to +125°C(74) -55 to +125°C(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Stored A Data to $\bar{B}$ Bus (653) Stored A Data to B Bus (654)	t <sub>PLH</sub> t <sub>PHL</sub>	5*	2.8	13.9	2.7	15.5	ns
Stored $\bar{B}$ Data to A Bus (653)	t <sub>PZL</sub>	5	2.8	13.9	2.7	15.5	ns
Stored B Data to A Bus (654)	t <sub>PLZ</sub>	5	3.4	16.9	3.2	18.5	ns
A Data to $\bar{B}$ Bus (653) A Data to B Bus (654)	t <sub>PLH</sub> t <sub>PHL</sub>	5	2.6	12.7	2.4	14.2	ns
$\bar{B}$ Data to A Bus (653)	t <sub>PZL</sub>	5	2.6	12.7	2.4	14.2	ns
B Data to A Bus (654)	t <sub>PLZ</sub>	5	3.2	15.7	3	17.2	ns
Select to Data (B Bus) (653/654)	t <sub>PLH</sub> t <sub>PHL</sub>	5	2.8	13.9	2.7	15.5	ns
Select to Data (A Bus) (653/654)	t <sub>PZL</sub> t <sub>PLZ</sub>	5	2.8 3.4	13.9 16.9	2.7 3.2	15.5 18.5	ns
3-State Enabling/ Disabling Time (B Bus) Bus to Output or Register to Output (653/654)	t <sub>PZL</sub> t <sub>PZH</sub> t <sub>PLZ</sub> t <sub>PHZ</sub>	5	2.8	13.9	2.7	15.5	ns
Off-State Enabling/ Disabling Time (A Bus) Bus to Output or Register to Output (653/654)	t <sub>PZL</sub> t <sub>PLZ</sub>	5	2.8	13.9	2.7	15.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—					pF
Min. (Valley) V <sub>OH</sub> (B Side) During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ @ 25°C				V
Input Capacitance	C <sub>i</sub>	—	—	10	—	10	pF
3-State Output Capacitance (B Side)	C <sub>o</sub>	—	—	15	—	15	pF
Off-State Output Capacitance (A Side)	C <sub>o</sub>	—	—	15	—	15	pF

\* Min. is @ 5.5 V

max. is @ 4.5 V

min. is @ 5.25 V for 0 to +70°C

max. is @ 4.75 V for 0 to +70°C

§C<sub>PD</sub> is used to determine the dynamic power consumption, per package.
$$P_D = V_{CC}^2 C_{PD} f_i + \sum V_{CC}^2 C_L f_o + V_{CC} \Delta I_{CC}$$

where  $f_i$  = input frequency  
 $f_o$  = output frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

**CD54/74AC653, CD54/74AC654**  
**CD54/74ACT653, CD54/74ACT654**

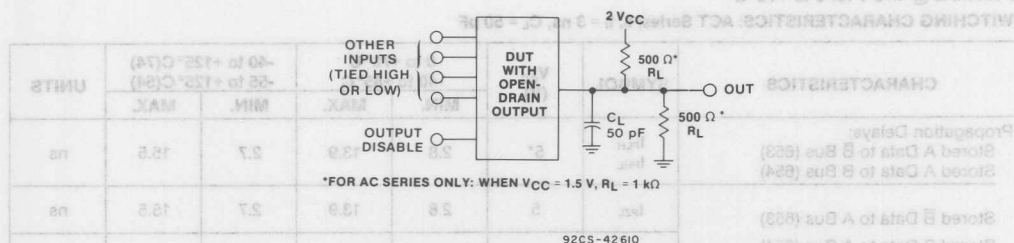
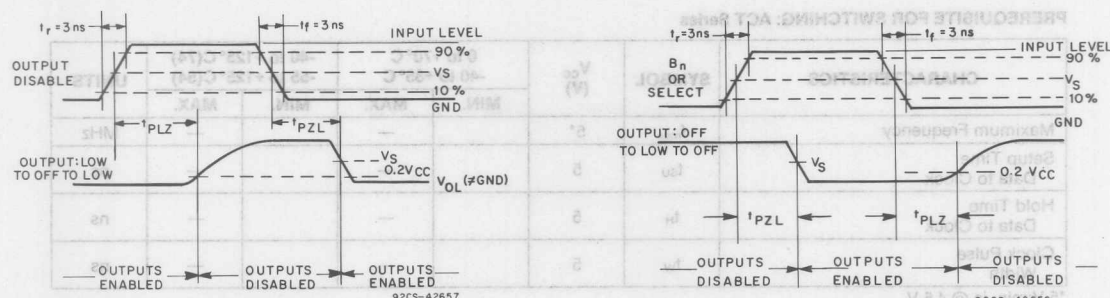


Fig. 3 - Open-drain propagation delay times and test circuit (A outputs).

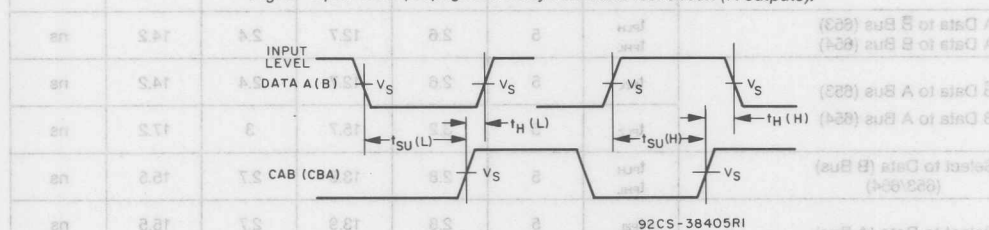
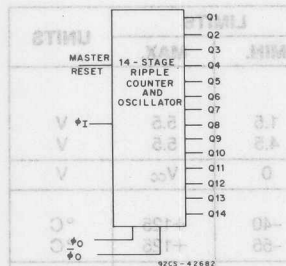


Fig. 4 - Data setup and hold times.

[illegible]

RECOMMENDED OPERATING CONDITIONS:  
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:



FUNCTIONAL DIAGRAM

## 14-Stage Binary Counter with Oscillator

### Type Features:

- Onboard oscillator
- Buffered inputs
- Common reset
- Negative edge clocking
- Typical  $f_{MAX} = 200 \text{ MHz}$  @  $V_{CC} = 5 \text{ V}$ ,  $C_L = 50 \text{ pF}$

The RCA CD/54/74ACT060 and CD54/74ACT060 each consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A Master Reset input is provided which resets the counter to the all-0's state and disables the oscillator. A high level on the MR line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of  $\phi_i$  (and  $\phi_o$ ). All inputs and outputs are buffered. Schmitt trigger action on the input-pulse line permits much slower rise and fall slew rates.

In order to achieve a symmetrical waveform in the oscillator section, the ACT7060 input pulse switchpoints are the same as in the AC7060; only the MR input in the ACT7060 has TTL switching levels.

The CD54ACT060 and CD54ACT060 are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74ACT060 and CD74ACT060 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small outline packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current ( $Q1$ ,  $Q2$ , and  $Q3$ )
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

$\phi_i$	MR	OUTPUT STATE
	L	No Change
	L	Advance to Next State
X	H	All Outputs are Low

H = high level (steady state)

L = low level (steady state)

X = don't care



# CD54/74AC7060 CD54/74ACT7060

Product Preview

## RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}^*$ : (For $T_A$ = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, $V_i$ , $V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$ : CD74 Types CD54 Types	-40 -55	+125 +125	°C °C
Input Rise and Fall Slew Rate, $dt/dv^\dagger$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V



$^\dagger$ Applicable for MR. Schmitt input on  $\phi_1$  line permits slower slew rates.

\*Unless otherwise specified, all voltages are referenced to ground.

## MAXIMUM RATINGS, Absolute-Maximum Values:

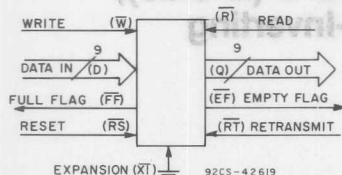
DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ): For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ): PACKAGE TYPE F	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING): At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

No Change	L	
Advance to Next State	L	
All Outputs are Low	H	X

H = high level (steady state)  
L = low level (steady state)  
X = don't care

# CD54/74AC7201, CD54/74AC7202 CD54/74ACT7201, CD54/74ACT7202



FUNCTIONAL DIAGRAM

## Parallel FIFO

CD54/74AC/ACT7201 - 512 x 9 Bit  
CD54/74AC/ACT7202 - 1024 x 9 Bit

### Type Features:

- Asynchronous and simultaneous read/writes in multiprocessing and rate-buffer applications
- Fully expandable by both word depth and/or bit width

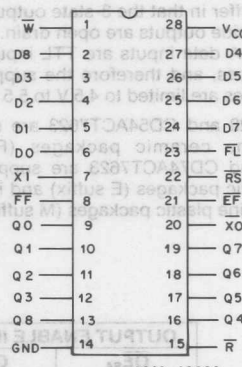
The RCA CD54/74AC7201, -7202 and CD54/74ACT7201, -7202 are dual-port memories that utilize RCA's new ADVANCED CMOS LOGIC technology. Data are loaded and emptied on a first-in, first-out (FIFO) basis. Full and empty flags are used to prevent data overflow and underflow, and expansion logic is provided for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers; no address information is required to load and unload data. Data is toggled in and out of the device through the use of Write (W) and Read (R) control pins.

The 9-bit wide data array allows control and parity bits to be used at the user's option. This device also features a Retransmit (RT) capability that allows for reset of the read pointer to its initial position when RT is pulsed LOW to allow for transmission from the beginning of data.

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Balanced propagation delays
- AC type features 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 8$  mA output drive current



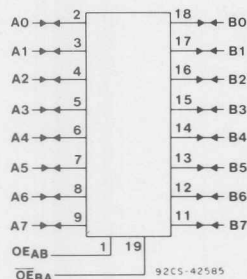
TERMINAL ASSIGNMENT

### RESET AND RETRANSMIT — SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	RS	RT	Xi	READ POINTER	WRITE POINTER	EF	FF
Reset	0	X	0	Location Zero	Location Zero	0	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X
Read/Write	1	1	0	Increment*	Increment*	X	X

\*Pointer will increment if flag is HIGH.

# CD54/74AC7623 CD54/74ACT7623



FUNCTIONAL DIAGRAM

## Octal-Bus Transceiver, 3-State (B Side), Open-Drain (A Side), Non-Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay:  
6 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

The RCA CD54/74AC7623 and CD54/74ACT7623 are octal-bus transceivers that utilize RCA's new ADVANCED CMOS LOGIC technology. They are non-inverting 3-state bidirectional transceiver-buffers that allow for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus depending on the logic levels of the Output Enable ( $OE_{AB}$ ,  $OE_{BA}$ ) inputs.

These devices are modified versions of the CD54/74AC/ACT623. They differ in that the 3-state outputs are on the B side only; the A side outputs are open drain. Another difference is that the A data inputs are TTL inputs for both the AC and ACT types, and therefore the supply-voltage and bus-voltage ranges are limited to 4.5 V to 5.5 V.

The CD54AC7623 and CD54ACT7623 are supplied in 20-lead dual-in-line ceramic packages (F suffix). The CD74AC7623 and CD74ACT7623 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix).

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power
- Balanced propagation delays
- AC type features balanced noise immunity at 30% of the supply on the B data inputs and Output Enable inputs
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

OUTPUT ENABLE INPUTS		OPERATION
$OE_{BA}$	$OE_{AB}$	
L	L	B DATA TO (OPEN-DRAIN) A BUS
H	H	A DATA (TTL) TO (3-STATE) B BUS
H	L	ISOLATION
L	H	B DATA TO (OPEN-DRAIN) A BUS, A DATA (TTL) TO (3-STATE) B BUS

H = High level, L = Low level

To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10k $\Omega$  to 1M $\Omega$  resistors.

# **MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_O$ ):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPE F	$-55$ to $+125^\circ\text{C}$
PACKAGE TYPE E, M	$-40$ to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{STG}$ )	$-65$ to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	$+300^\circ\text{C}$

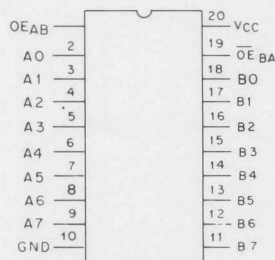
\*(For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.)

## **RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ †:			
(For $T_A$ = Full Package-Temperature Range)			
AC Types	4.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I, V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$ :			
CD74 Types	$-40$	$+125$	$^\circ\text{C}$
CD54 Types	$-55$	$+125$	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 4.5 V to 5.5 V (AC Types Except B Inputs)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types and B Inputs)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.



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## **TERMINAL ASSIGNMENT**

# CD54/74AC7623 CD54/74ACT7623

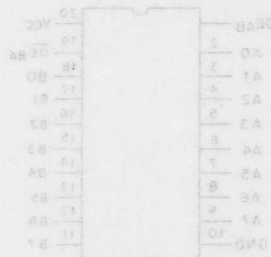
## STATIC ELECTRICAL CHARACTERISTICS: AC Series (Modified)

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage ■	V <sub>IH</sub>			5.5	3.85	—	3.85	—	3.85	—	V
Low-Level Input Voltage ■	V <sub>IL</sub>			5.5	—	1.65	—	1.65	—	1.65	V
High-Level Output Voltage (B Side)	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		#	-24	4.5	3.94	—	3.8	—	3.7	—	
		*	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		#	24	4.5	—	0.36	—	0.44	—	0.5	
		*	75	5.5	—	—	—	1.65	—	—	
		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State or Off-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

■For "A" side  $V_{IH}$  and  $V_{IL}$ , refer to ACT limits.



TERMINAL ASSIGNMENT



# CD54/74AC7623 CD54/74ACT7623

## STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
					+25		0 to +70 -40 to +85		-40 to +125(74) -55 to +125(54)		
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V <sub>IL</sub>			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage (B Side)	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		#	-24	4.5	3.94	—	3.8	—	3.7	—	
		*	-75	5.5	—	—	3.85	—	—	—	
		*	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		#	24	4.5	—	0.36	—	0.44	—	0.5	
		*	75	5.5	—	—	—	1.65	—	—	
		*	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State or Off-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>									
		V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Supply Current per Input Pin											
TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability for 74AC/ACT Series, 75 ohms for 54AC/ACT Series.

## ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
An, Bn	0.83
OE <sub>BA</sub>	0.64
OE <sub>AB</sub>	0.15

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC7623 CD54/74ACT7623

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125(74) -55 to +125(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: A Data to B Bus	$t_{PLH}$ $t_{PHL}$	5*	2	9.8	1.9	10.9	ns
B Data to A Bus	$t_{PZL}$	5	1.8	8.6	1.7	9.6	ns
	$t_{PLZ}$	5	2.5	12	2.4	13.4	ns
Output Enable or Disable to Output 3-State (B Side)	$t_{PZH}$	5	2.5	12	2.4	13.4	ns
	$t_{PLZ}$	5	2.5	12	2.4	13.4	ns
	$t_{PHZ}$	5	2.5	12	2.4	13.4	ns
Off-State Enabling, Disabling Times (A Side)	$t_{PZL}$ $t_{PLZ}$	5	2.5	12	2.4	13.4	ns
Power Dissipation Capacitance	$C_{PD}\S$	—	—	—	—	—	pF
Min. (Valley) $V_{OH}$ (B Side) During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OHV}$ See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OLP}$ See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	$C_i$	—	—	10	—	10	pF
3-State Output Capacitance (B Side)	$C_o$	—	—	15	—	15	pF
Off-State Output Capacitance (A Side)	$C_o$	—	—	15	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	$V_{CC}$ (V)	0 to +70°C -40 to +85°C		-40 to +125(74) -55 to +125(54)		UNITS
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: A Data to B Bus	$t_{PLH}$ $t_{PHL}$	5*	2	9.8	1.9	10.9	ns
B Data to A Bus	$t_{PZL}$	5	2	9.8	1.9	10.9	ns
	$t_{PLZ}$	5	2.7	13.2	2.5	14.7	ns
Output Enable or Disable to Output 3-State (B Side)	$t_{PZH}$	5	2.7	13.2	2.5	14.7	ns
	$t_{PLZ}$	5	2.7	13.2	2.5	14.7	ns
	$t_{PHZ}$	5	2.7	13.2	2.5	14.7	ns
Off-State Enabling, Disabling Times (A Side)	$t_{PZL}$ $t_{PLZ}$	5	2.7	13.2	2.5	14.7	ns
Power Dissipation Capacitance	$C_{PD}\S$	—	—	—	—	—	pF
Min. (Valley) $V_{OH}$ (B Side) During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OHV}$ See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OLP}$ See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	$C_i$	—	—	10	—	10	pF
3-State Output Capacitance (B Side)	$C_o$	—	—	15	—	15	pF
Off-State Output Capacitance (A Side)	$C_o$	—	—	15	—	15	pF

\*5 V: min. is @ 5.5 V  
max. is @ 4.5 V

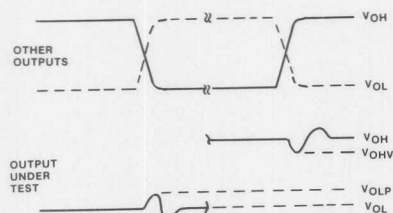
5 V: min. is @ 5.25 V for 0 to +70°C  
max. is @ 4.75 V for 0 to +70°C

$\S C_{PD}$  is used to determine the dynamic power consumption, per channel.

For AC series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

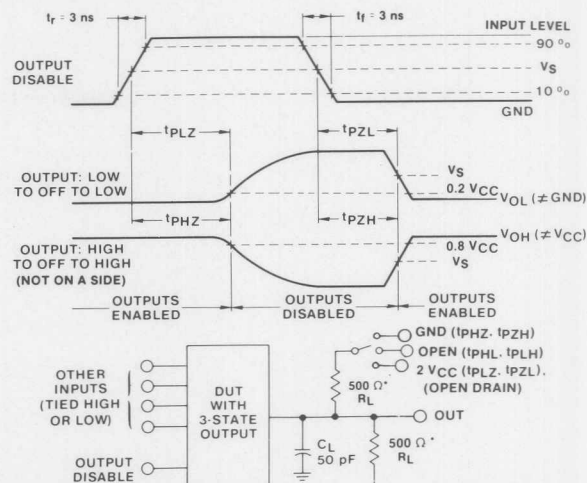
For ACT series:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
1.  $V_{OHV}$  and  $V_{OLP}$  ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
  2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:  
 $PRR \leq 1$  MHz,  $t_r = 3$  ns,  $t_f = 3$  ns, SKEW  $\leq 1$  ns.
  3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.  
 IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH  $0.1 \mu F$  CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

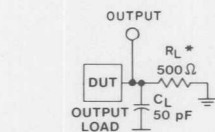


\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5$  V,  $R_L = 1$  k $\Omega$

92CM-42609

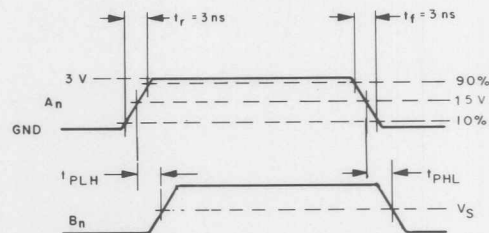
Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Three-state propagation delay times and test circuit.



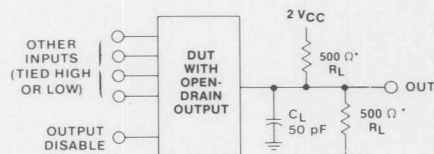
\*FOR AC SERIES ONLY: WHEN  
 $V_{CC} = 1.5$  V,  $R_L = 1$  k $\Omega$

92CS-42589



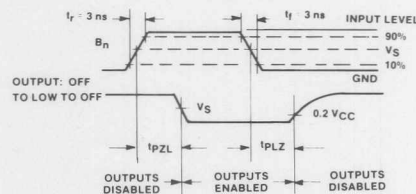
92CS-42608

Fig. 3 - Propagation delay times and test circuit (A Data to B Bus).



\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5$  V,  $R_L = 1$  k $\Omega$

92CS-42610



92CS-42607

Fig. 4 - Open-drain propagation delay times and test circuit (B Data to A Outputs).

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$

# CD5474AC7623 CD5474AC7623

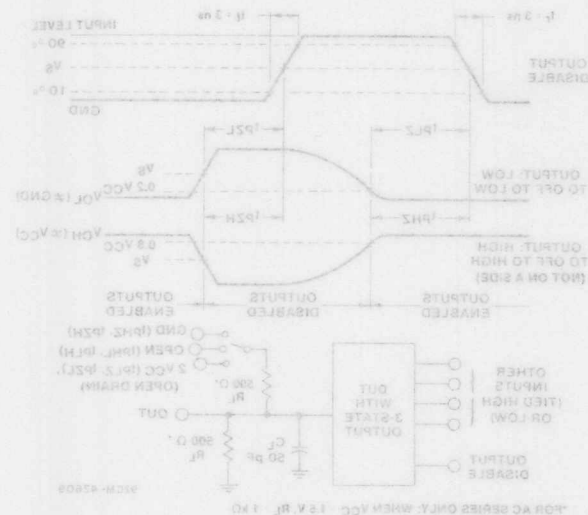


Fig. 2 - Three-state propagation delay times and test circuit.

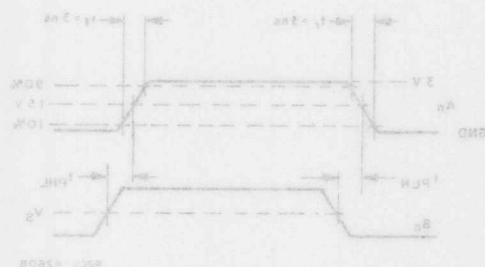


Fig. 3 - Propagation delay times and test circuit (A Data to B Bus).

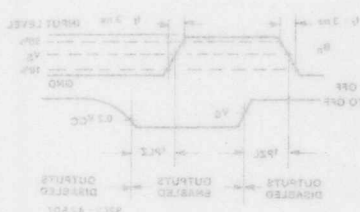


Fig. 4 - Open-drain propagation delay times and test circuit (B Data to A Outputs).

CD5474AC	CD5474AC
Input Level	V <sub>cc</sub>
Input Switching Voltage, V <sub>s</sub>	0.5 V <sub>cc</sub>
Output Switching Voltage, V <sub>s</sub>	0.5 V <sub>cc</sub>

## PARAMETER MEASUREMENT INFORMATION

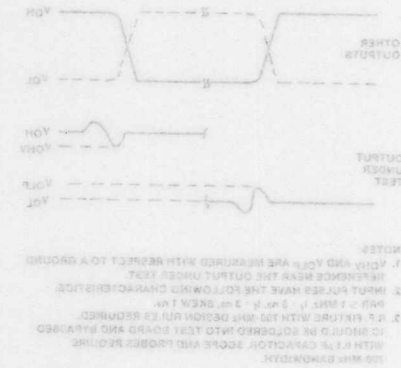


Fig. 1 - Simultaneous switching transient waveforms.

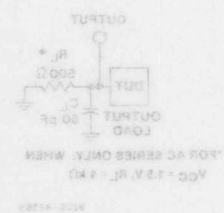
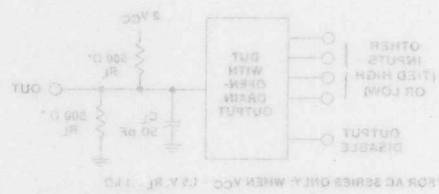


Fig. 5 - Propagation delay times and test circuit (A Data to B Bus).







# Total Lot Screening (A - 100% Testing)

Screening Tests	Conditions	MIL-STD-883		Screening Levels /3A	Notes
		Method	Conditions		
Assembly Precap Visual		2010	B	X	
Preconditioning					
Stabilization Bake	24 hrs. min. at 150°C	1008	C	X	
Temperature Cycling	10 Cycles	1010	C	X	
Centrifuge	Y <sub>1</sub> direction only	2001	E	X	
Fine Leak	—	1014	A or B	X	
Gross Leak	—	1014	C	X	
Test and Burn-in					
Initial Test	—	—	—	X	
Static Burn-in	120 hrs. @ 135°C	1015	B	X	1
Final Electrical					
Static Electrical (DC)	25°C	—	—	X	2, 3
	-55°C	—	—	X	
	+125°C	—	—	X	
	25°C, -55°C, +125°C	—	—	X	
Dynamic Electrical (AC)					
Group A	—	—	X	X	4

- Notes:**
1. Alternate time/temperature regression used per Method 1015.
  2. All electrical testing per parameters shown in individual device data sheets.
  3. PDA = 5%, one reburn allowed at 3%.
  4. Sample test performed per Method 5005 of MIL-STD-883.

## Manufacturing and Conformance Testing

Characteristic	/3A <sup>1</sup>
SERIES	AC, ACT
PACKAGE	F
DIE ATTACH	EUTECTIC
LEAD FINISH	SOLDER DIP
MANUFACTURING LOCATION	OFF-SHORE
SCREENING	METHOD 5004
CONFORMANCE TESTS	
GROUP A	METHOD 5005
CLASS B, GROUP B <sup>2</sup>	METHOD 5005
CLASS B, GROUP C	METHOD 5005
GROUP D	METHOD 5005
DATA SUPPLIED	
C OF C <sup>3</sup>	YES

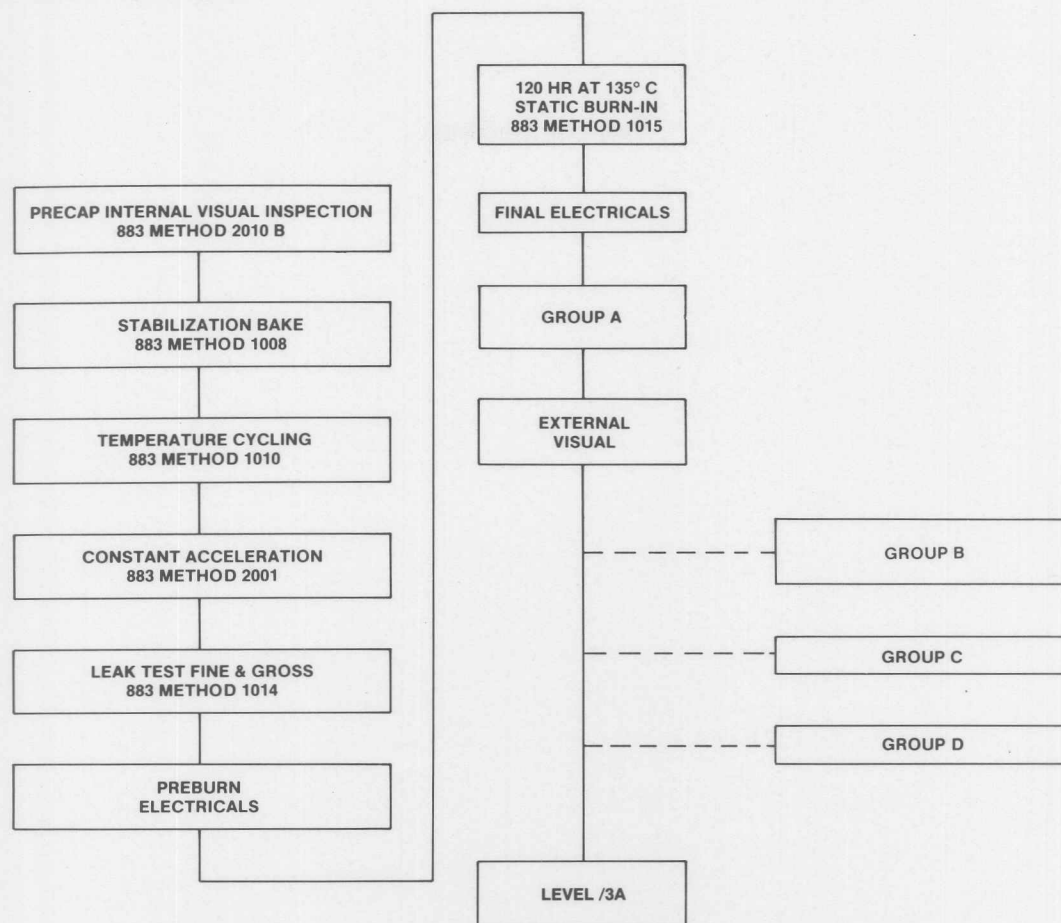
### NOTES:

1. Slash 3A meets MIL-STD-883 Class B.
2. For Slash 3A Series, Group B will be run on each inspection lot representing 6 weeks of product.
3. Certificate of compliance (C of C) signed by RCA representative provides identity and customer order number, and lists and certifies tests, methods and conditions per MIL-STD-883. Group A and B attributes data will be supplied.

## ACL DESC Surface-Mount Devices Cross-Reference Guide

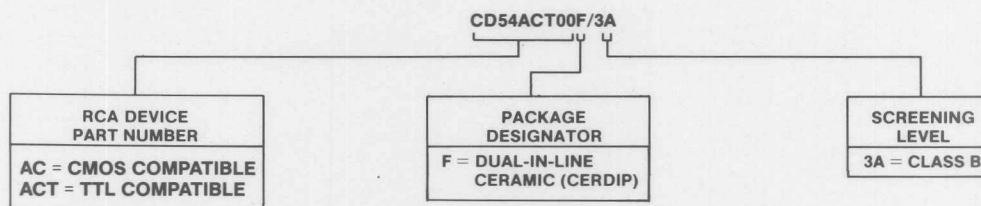
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CD54AC241F3A	5962-8755101RA	CD54AC20F3A	5962-8761301CA
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CD54ACT138F3A	5962-8755401EA	CD54AC139F3A	5962-8762301EA
CD54AC373F3A	5962-8755501RA	CD54AC138F3A	5962-8762201EA
CD54ACT373F3A	5962-8755601RA	CD54AC540F3A	5962-8769501RA
CD54AC08F3A	5962-8761501CA	CD54AC253F3A	5962-8769301EA
CD54AC14F3A	5962-8762401CA	CD54AC151F3A	5962-8769101EA
CD54AC32F3A	5962-8761401CA	CD54AC251F3A	5962-8769201EA
CD54AC04F3A	5962-8760901CA	CD54ACT245F3A	5962-8766301RA
CD54AC10F3A	5962-8761001CA	CD54AC374F3A	5962-8769401RA

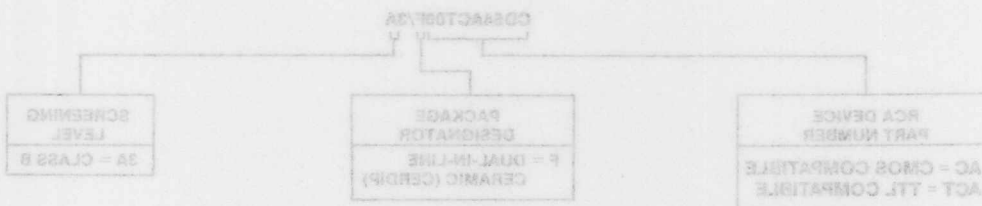
## Product Flow Diagram



RCA HIGH-RELIABILITY LEVEL /3A 54AC/ACT IC'S

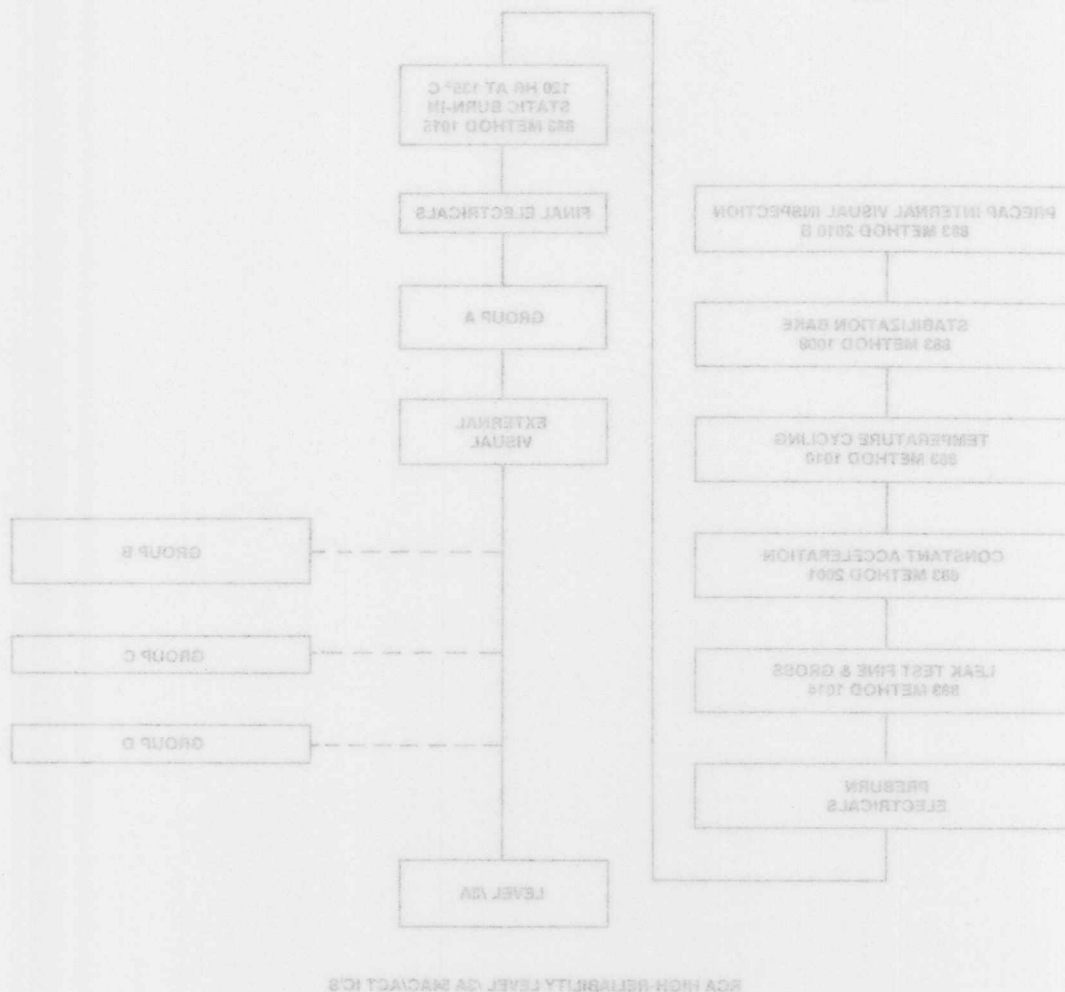
## Guide to the Reliability Class and Package of RCA High-Reliability 54AC/ACT Integrated Circuits





## Screening

Product Flow Diagram



## Using Advanced CMOS Logic in a VME Data Bus System

J. Nadozski and Alan Kalish

and two external I/O cards. Table I contains more detailed information on the system components. The configuration of the system places the three cards evenly through the rack. The CPU card is at one end, the 8-port card at the other, and the external CMOS RAM card is spaced evenly in the middle. Fig. 1 illustrates the configuration of the system in a block diagram.

Table I - System Components

Manufacturer	Model No.	Function
Force Computer	88030	CPU with 512K Memory
Force Computer	88030	CPU with 512K Memory
Force Computer	88030	CPU with 512K Memory
Force Computer	88030	CPU with 512K Memory
Force Computer	88030	CPU with 512K Memory
Force Computer	88030	CPU with 512K Memory
Force Computer	88030	CPU with 512K Memory
Force Computer	88030	CPU with 512K Memory
Force Computer	88030	CPU with 512K Memory
Force Computer	88030	CPU with 512K Memory

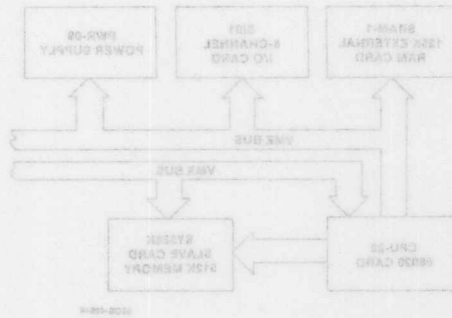


Fig. 1 - Block diagram of VME system.

### STANDARD BIPOLAR LOGIC SYSTEM - UNMODIFIED

Tests performed on the Operating System. The power on the 5-volt supply is monitored, and the system's major waveforms are recorded and compared to the published standards of the manufacturer. Built-in benchmark timing tests are used to verify system timing, access timing, and communication ability between the cards. Built-in tests, designed by the manufacturer, assure that the system is operating within the specifications. These tests allow the comparison of the unmodified system (which contains bipolar FAST and LSTTL) to the modified system (which contains ACL and High-Speed CMOS). The correlation of these timing tests is very important to the validity of this conversion experiment.

### SUMMARY

Advanced CMOS Logic (ACL) and High-Speed CMOS (HSP) are ideal for use in VME or any other system. Their benefits of low power consumption, high speed, excellent noise immunity, and wider operating-temperature range are important in system designs. This note describes the performance of RCA's Advanced CMOS Logic and High-Speed CMOS in a VME system computer. The performance of the system with CMOS is compared to the unmodified off-the-shelf bipolar computer. ACL and High-Speed CMOS logic show greater tolerance to input signal levels, lower power consumption, than their bipolar counterparts. This demonstrates that a system conversion to CMOS saved 8 watts of a total of 28 watts dissipated by the bipolar system without affecting system timing or operation.

### INTRODUCTION

One of the biggest problems in any system is power and heat dissipation. These factors commonly cause the typical system to be larger and more expensive than the designer wishes. But now, with the advent of High-Speed CMOS and Advanced CMOS Logic, the system designer has an alternative to power-hungry bipolar logic.

This note describes the benefits of using Advanced CMOS Logic from RCA in a VME system computer. The VME system was chosen over all others (e.g., multiprocessor, bus, and S-100 bus) as an excellent candidate because of the large amount of glue logic used in it, and because this type of system would benefit most from the replacement of its bipolar glue parts, largely FAST and LSTTL. Advanced CMOS Logic has a drive capability of  $\pm 24$  mA at 0.5V. The VME specification requires that drive logic be capable of driving 64 mA over a number of backplanes. Because of the lower drive current of the ACL logic, the number of backplanes is limited in this experiment to one VME and one VMX backplane, which have terminations of 330 and 470 ohms at each end. This limitation, imposed by drive current, should not prevent the user from reaping the benefits of replacing his bipolar logic with Advanced CMOS Logic, because in many systems only a few paths of many need adhere to the drive-current specification. As highlighted in this paper, the advantages of using ACL are: much lower standby power, better reliability due to lower junction temperature and, because of the power savings, lower cost.

The data for this note was collected first on the unmodified system, which contains bipolar logic (FAST and LSTTL). The system was tested in several operating modes. The 5-volt power supply was monitored with a clamp-on current probe, and waveform integrity was recorded. The system consists of a double-height 19-inch VME rack with power supply, both VME and VMX PCB buses, a system CPU controller with its internal memory,

# Using Advanced CMOS Logic in a VME Data Bus System

J. Nadolski and Alan Kalish

## SUMMARY

Advanced CMOS Logic (ACL) and High-Speed CMOS (74 types) are ideal for use in VME or any other system. Their benefits of low power consumption, high speed, excellent noise immunity, and wider operating-temperature range are important in system designs. This Note describes the performance of RCA's Advanced CMOS Logic and High-Speed CMOS in a VME system computer. The performance of the system with CMOS is compared to the unmodified off-the-shelf bipolar computer. ACL and High-Speed CMOS logic show greater tolerance to induced noise, and lower power consumption, than their bipolar equivalents. Data demonstrates that a system conversion to CMOS saved 9 watts of a total of 28 watts dissipated by the bipolar system without affecting system timing or operation.

## INTRODUCTION

One of the biggest problems in any system is power and heat dissipation. These factors commonly cause the typical system to be larger and more expensive than the designer wishes. But now, with the advent of High-Speed CMOS and Advanced CMOS Logic, the system designer has an alternative to power-hungry bipolar glue logic.

This Note describes the benefits of using Advanced CMOS Logic from RCA in a VME system computer. The VME system was chosen over all others (e.g., multibus, standard bus, and S-100 bus) as an excellent candidate because of the large amount of glue logic used in it, and because this type of system would benefit most from the replacement of its bipolar glue parts, largely FAST and LSTTL. Advanced CMOS Logic has a drive capability of  $\pm 24$  mA at 0.5V. The VME specification requires that drive logic be capable of driving 64 mA over a number of backplanes. Because of the lower drive current of the ACL logic, the number of backplanes is limited in this experiment to one VME and one VMX backplane, which have terminations of 330 and 470 ohms at each end. This limitation, imposed by drive current, should not prevent the user from reaping the benefits of replacing his bipolar logic with Advanced CMOS Logic, because in many systems only a few parts of many need adhere to the drive-logic specification. As highlighted in this paper, the advantages of using ACL are: much lower standby power, better reliability due to lower junction temperature and, because of the power savings, lower cost.

The data for this Note was collected first on the unmodified system, which contains bipolar bus interface logic (FAST and LSTTL). The system was tested in several operating modes. The 5-volt power supply was monitored with a clamp-on current probe, and waveform integrity was recorded. The system consists of a double-height 19-inch VME rack with power supply, both VME and VMX PCB buses, a system CPU controller with its internal memory,

and two external I/O cards. Table I contains more detailed information on the system components.

The configuration of the system places the three cards evenly through the rack. The CPU card is at one end, the 6-port card is at the other, and the external CMOS RAM card is spaced evenly in the middle. Fig. 1 illustrates the configuration of the system in a block diagram.

Table I - System Components

Manufacturer	Model No.	Function
Force Computer	CPU-20	68020 CPU with 512K Memory
Force Computer	SRAM-1	128K CMOS RAM Card
Force Computer	SIO-1	6 I/O Serial Port
Force Computer	MOTH-12A	VME PCB Bus
Force Computer	MOTH-12E	VMX PCB Bus
Force Computer	PWR-09A	Power Supply

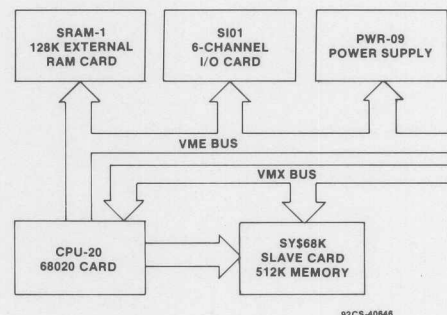


Fig. 1 - Block diagram of VME system.

## STANDARD BIPOLAR LOGIC SYSTEM - UNMODIFIED

### Tests Performed on the Operating System

The power on the 5-volt supply is monitored, and the system's major waveforms are recorded and compared to the published standards of the manufacturer. Built-in benchmark timing tests are used to verify system timing, access timing, and communication ability between the cards. Built-in tests, designed by the manufacturer, assure that the system is operating within the specifications. These tests allow the comparison of the unmodified system (which contains bipolar FAST and LSTTL) to the modified system (which contains ACL and High-Speed CMOS). The correlation of these timing tests is very important to the validity of this conversion experiment.



## ICAN-8640

**Comparison Tests** - The following tests are used to compare the operation of the system before and after the conversion of the glue logic:

1. Benchmark Test 1 - Decrement long word in memory 10M times.
2. Benchmark Test 2 - Pseudo DMA 1K bytes 50K times.
3. Benchmark Test 3 - Substring character search 100K times.
4. Benchmark Test 4 - Bit test/set/reset 100K times.
5. Benchmark Test 5 - Bit matrix transposition 100K times.
6. Benchmark Test 6 - Cache test—128K program executed 1K times. (This test can only be performed on the main CPU memory because of the memory requirements.)
7. Monitoring the VME system clock.
8. Monitoring the major handshaking signals on the bus (DTACK, DATA VALID, DS"A" and DS"B") and comparing the results to the specifications both before and after conversion.
9. The 5-volt power supply is monitored with a clamp-on current probe to observe the change in both standby and operating power on the VME and VMX bus.
10. The bus waveforms are monitored to observe the signal reflections on the bus.
11. All critical waveforms are monitored for their signal reflections.
12. A test macro program is generated and its execution time is recorded and compared.

The tests were chosen to be as simple as possible (allowing the system designer to easily evaluate the modification) but still provide accurate testing of the system.

#### Standard Unmodified System Benchmarks and Specifications

Table II contains the critical timing specifications required and used in the test. Table III contains the results of the benchmark timing tests.

**Table II - Critical Timing Specifications**

Signal	Critical Specs.	Observed Specs.
Sys Clk	16.0000 MHz	16.0102 MHz
DS0 to DS1 skew	20 ns max	3 ns
Data Valid to DTACK	0 ns min	40 ns
AS to BTACK	20 ns min	30 ns

**Table III - Results of Benchmark Timing Tests**

Test	Timing Results (seconds)
Main Bd.	
Bench No.	
1	10.79
2	13.90
3	11.91
4	3.71
5	11.29
6	21.64

The system clock is shown in Fig. 2. The top waveform is monitored at the driver output while the bottom waveform is the system clock signal at the very end of the bus (at the I/O port card). All three cards are in the system, and signal reflections can be seen as three bumps when the signal is low. Each reflection is about 5 ns wide and about 0.75 volt above ground. As each card is removed, the number of reflections and the loading factor is reduced. Fig. 3 illustrates that there are less reflections and that the signal integrity has improved.

Fig. 4 shows the same effect, but with only the main card in the system. These reflections are from each input and the bus. If the reflection voltage exceeds the TTL switching threshold, false triggering will occur and system operation will be hampered.

Fig. 5 illustrates the signals of DS0 to DS1. Fig. 6 illustrates DATA VALID to DTACK. Fig. 7 illustrates AS to BTACK. These signals are detailed in Table III.

#### Power

The unmodified system consists almost entirely of bipolar-type logic: TTL, LSTTL and FAST, which are glue logic, plus many bipolar LSI and VLSI parts. Another large user of power is the VME resistor terminations, which are at either end of the bus. The system uses a full 32 bits with the option of either a 16 or 32-bit data bus. There is also the VMX bus, which extends the system for 32-bit operation and contains the same resistor terminations as the VME bus. A typical VME board is multilayer (a requirement because of the number of connections and the huge amount of power required to operate the circuits). Table IV shows the amount of power the unmodified system requires and each board's contribution.

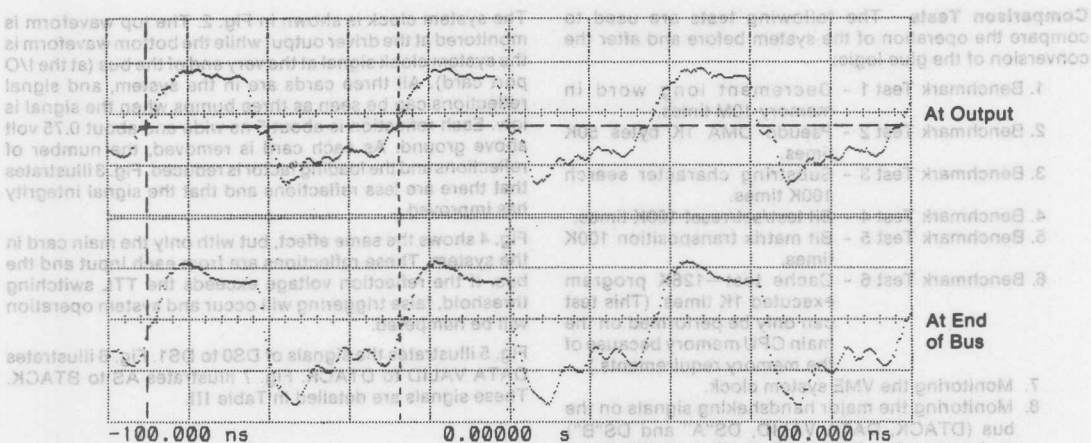
**Table IV - System Power and Board Contribution**

Item	Power - 5V (Watts)	
	VME	VMX
CPU-20	14.25	7.05
SRAM-1	2.95	NA
SI/01	3.65	NA
Total	20.85	7.05
Total Operating Power (Data Access)	21.25	8.99
Total Power - 5V Supply: 27.9 Watts		

#### Unmodified-System Summary

The above tests and data show that the present system is in good working order, and that it follows the manufacturer's specifications. All of the above data will be used to compare the operation, performance and system integrity to the modified system (bipolar logic replaced with ACL and High-Speed CMOS). The unmodified system uses a very large amount of power. The modified system will reduce both the standby and operating power through the replacement of the glue logic; the LSI and VLSI parts in the system cannot be changed.

## ICAN-8640



Ch. 1 = 2.000 volts/div  
 Ch. 2 = 2.000 volts/div  
 Timebase = 20.0 ns/div  
 Ch. 1 Parameters

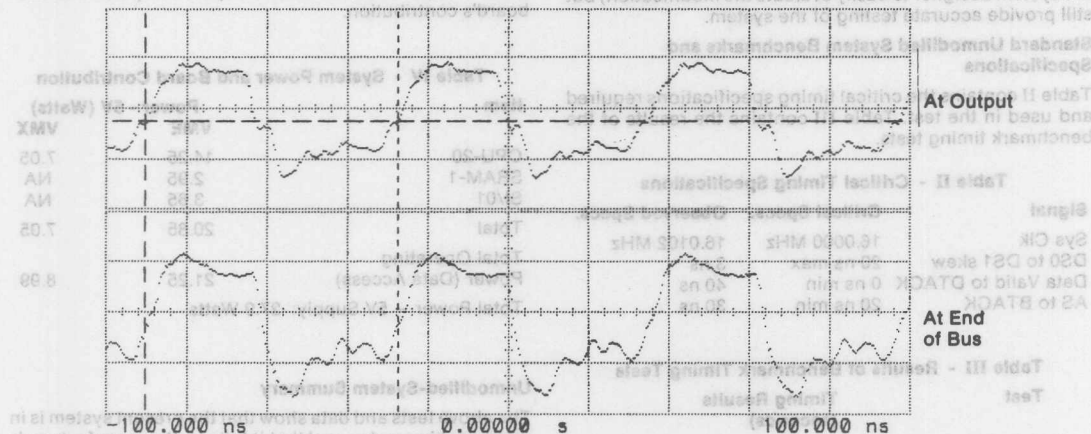
Offset = 2.000 volts  
 Offset = 2.000 volts  
 Delay = 0.00000 s  
 Freq. = 16.0051 MHz

Fig. 2 - Signal reflections, 3 cards.

The system designer is responsible for ensuring that the system is properly terminated. The system uses a full 32-bit data bus. There is also the VMX bus, which extends the system for 32-bit operation and contains the same resistor terminations as the VME bus. A typical VME board is multilayer (a requirement because of the number of connections and the huge amount of power required to operate the circuit). Table IV shows the amount of power the unmodified system requires and each

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Ch. 1 = 2.000 volts/div  
 Ch. 2 = 2.000 volts/div  
 Timebase = 20.0 ns/div  
 Ch. 1 Parameters

Offset = 2.000 volts  
 Offset = 2.000 volts  
 Delay = 0.00000 s  
 Freq. = 16.0051 MHz

Fig. 3 - Signal reflections, 2 cards.

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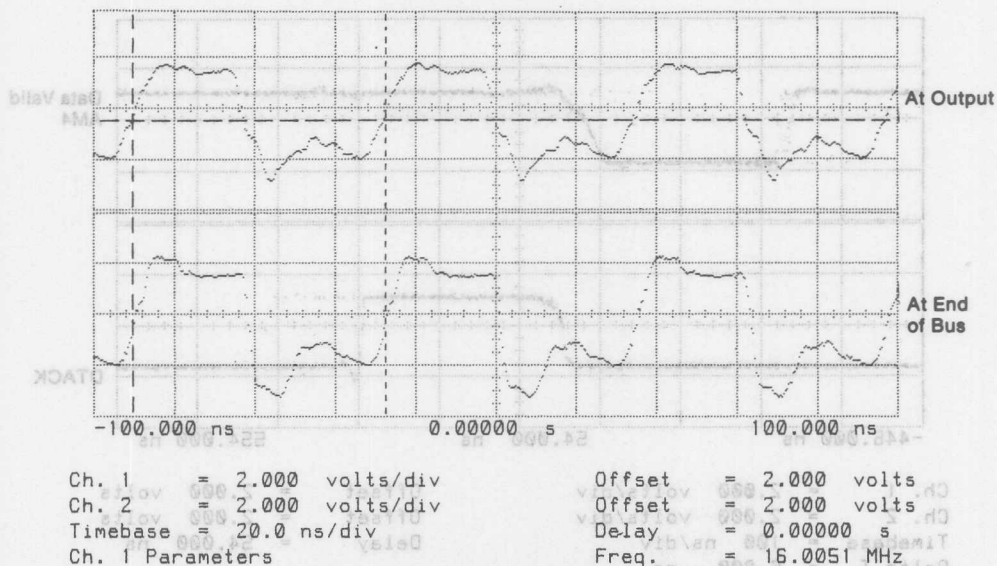


Fig. 4 - Signal reflections, 1 card.

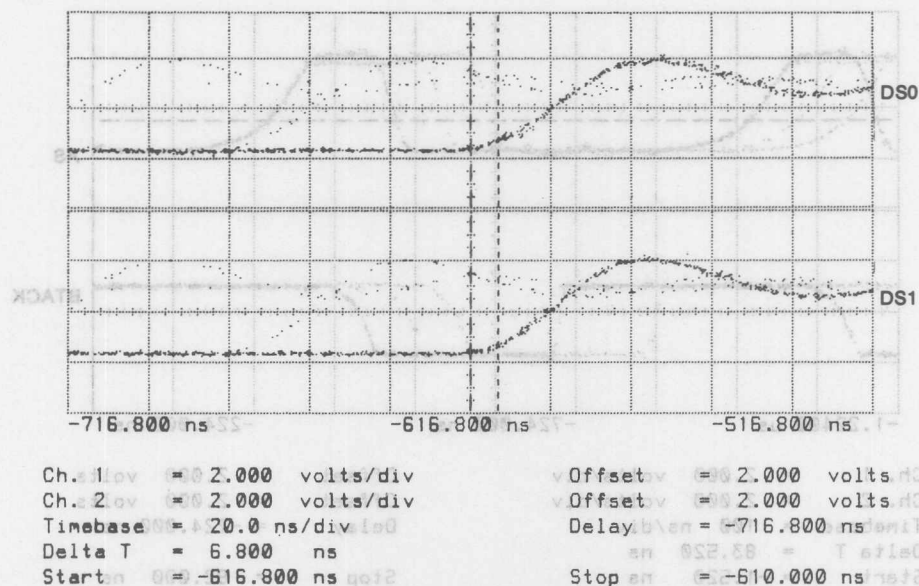


Fig. 5 - DS0 to DS1.

## ICAN-8640

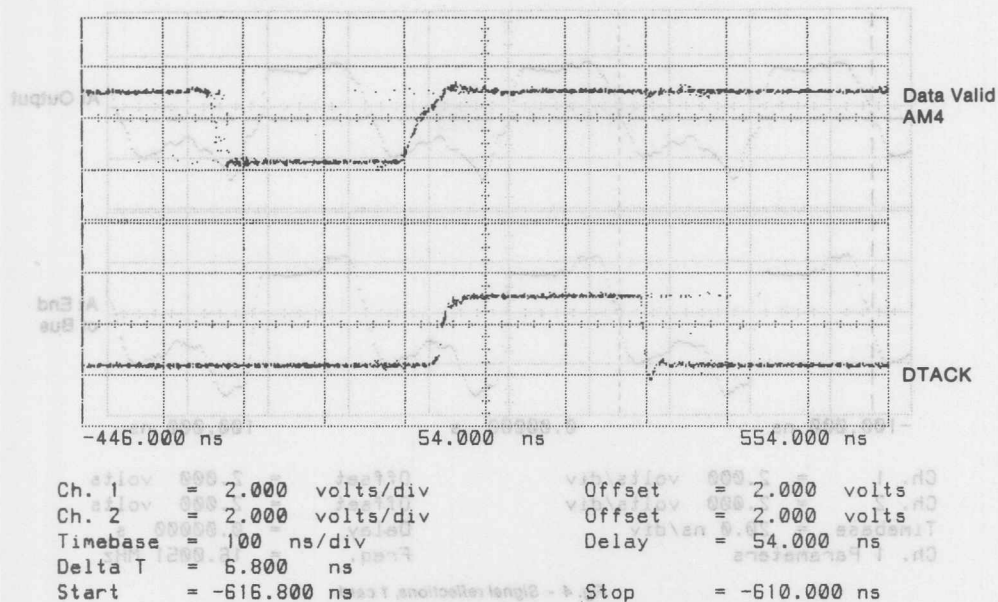


Fig. 6 - Data valid to DTACK.

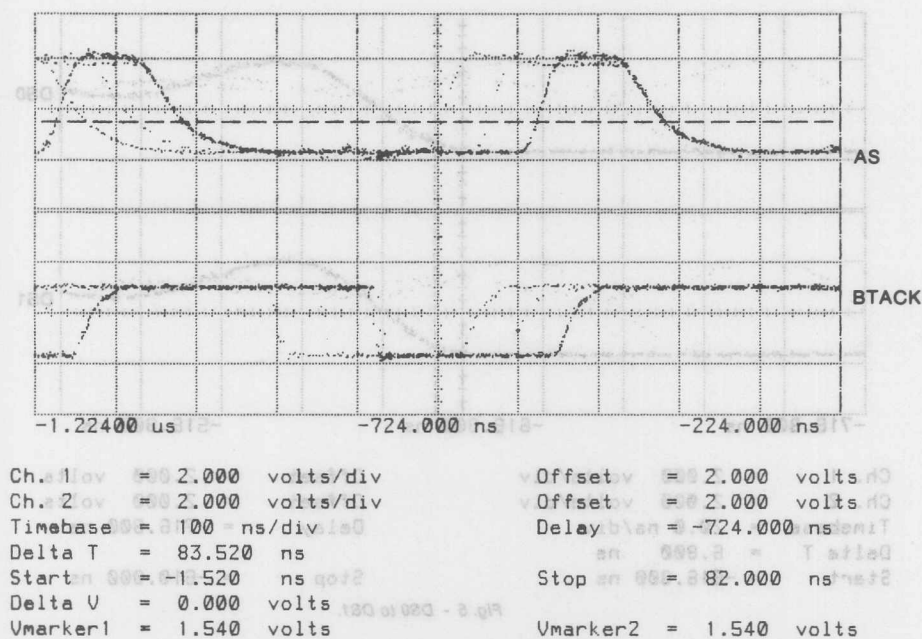


Fig. 7 - AS to BTACK.



## ICAN-8640

## MODIFIED SYSTEM DATA

This section of the Note deals with the replacement of the bipolar glue logic with Advanced CMOS Logic and High-Speed CMOS parts. It consists of a comparison of timing, signal integrity, waveforms, and power savings of the unmodified system with the modified one.

The same tests as those used in the unmodified system will be performed and their results recorded for comparison. The test results must be within the manufacturer's specifications to prove the modification successful.

## Modification Procedure

In replacing the glue logic, the specifications of the ACL and the High-Speed CMOS parts must be met. The system schematic must be reviewed, and only those parts that can be operated within specification can be substituted. The VME bus specification states that each driver must be able to sink a total of 64 mA at 0.5V. ACL can only sink 24 mA at 0.4V. For the purpose of this experiment, the VME bus in the system is limited to 1 backplane and terminations at either end only. This restriction keeps the operation to within the limits of ACL and allows the replacement to be carried out.

Each card is reviewed and modified with the correct logic. FAST is replaced with AC, and LSTTL is replaced with HCT High-Speed CMOS logic. The AC type logic is used because the signal inputs are at CMOS levels, or unloaded TTL outputs pulled up to at least 4.25, which is above the  $V_{IH}$  of 3.5V of the AC specification, and most of the glue logic is associated with the data buses. HCT High-Speed CMOS is used to replace LSTTL because of its ability to switch on TTL levels; most of the LSTTL ICs interface to bipolar LSI and VLSI.

ALS is also present in the system, mainly in the external card's VME bus interface. The ALS 645-1 has a higher current-sink capability than normal ALS. For the purpose of this paper, the ALS 645-1 and 641-1 are being replaced by the AC245 and the AC241. These AC parts have the same pinout and function with the increase in speed of ACL. The ALS drivers are directly connected to the VME and VMX buses, which for this experiment are being limited to the restriction stated above.

## Standard Modified System Benchmarks and Specifications

Table V contains the critical timing specifications monitored, and compares them to the unmodified system. Table VI contains the results of the benchmark timing tests. The above tests show that there are few or no timing changes between the modified and unmodified units. The only difference, which should not effect system timing, is that CMOS logic will give the user a more even propagation delay than bipolar logic, and a larger output-voltage swing.

Table V - Critical Timing Specifications

Signal	Critical Specs.	Observed Specs.
Sys Clk	16.0000 MHz	16.0359 MHz
DS0 to DS1 Skew	20 ns max	2.5 ns
Data Valid to DTACK	0 ns min	40 ns
AS to BTACK	20 ns min	29 ns

Table VI - Results of Benchmark Timing Tests

Test (Bench No.)	Timing Results (seconds)
1	10.79
2	13.90
3	11.92
4	3.71
5	11.29
6	21.65

## Waveforms

The system clock is shown in Fig. 8. The top waveform is monitored at the driver output, and the bottom one at the end of the bus (I/O card). All three cards are in the system, and the signal reflections from each card can be observed in the waveform during a low. The output voltage swing is higher due to the rail-to-rail swings of the CMOS technology. The signal integrity is similar to that of the unmodified unit. Each reflection can be seen, as mentioned above. Fig. 9 shows the system clock with only two cards present.

Fig. 10 shows the clock with only the main card present in the system. The clock signal has balanced high and low pulse widths. By using logic with CMOS thresholds, the noise margin of the bus and the system can be improved. Noise immunity in a TTL-type logic system is limited because of the lower switching thresholds. The unmodified system noise reflections approach the 0.8V TTL logic-low window.

With CMOS input devices, the typical 50% switching threshold provides the designer with a larger noise window than the TTL types. The larger CMOS signal output is thought to produce a larger EMI, RFI, and dv/dt than the signal output which TTL logic produces. Observations in this system show that the total RFI and EMI is about the same because of the lower power consumption, which is discussed in the next section.

## Power

The modified system contains a total of 51 Advanced CMOS Logic and 21 High-Speed CMOS parts. For the sake of simplicity, the VME and VMX terminations are left the same. In a VME system which, basically, is only active on the bus when communicating, the standby power consumption is very high because of the large quiescent current required by the bipolar logic. The modified system replaces this logic with CMOS, which has almost no quiescent current requirements, it only consumes power when switching. Even though the bipolar LSI and VLSI cannot be replaced, there is still a substantial power reduction in the system. Table VII shows the power measured in the system after the conversion.

## MODIFIED SYSTEM SUMMARY

The modified system demonstrates the many reasons for using CMOS instead of power-hungry bipolar logic. Overall system operations and timing are not effected by the change, but power dissipation clearly drops. The significant power reduction highlighted by the above data clearly points out the reasoning behind and advantages to a conversion to CMOS logic. The conclusion of all of the above data is that CMOS logic (ACL and High-Speed CMOS) is far superior in standby power dissipation, noise margin, and reliability to bipolar types, and should be the first choice in system replacement or new designs. Moreover, the VME and VMX buses, which require a large power dissipating termination, should be redefined for use with CMOS logic and to reduce power use in systems, thereby improving reliability and lowering system cost.



Timing Results		No. of ICs Replaced			Power (5V) (Watts)		Savings over Bipolar (Watts)	
Item	(sec)	FAST	LSTTL	ALS				
CPU-20	10.79	30	0	7	VME: 9.9	VMX: 4.35		
	5.71	1	6	7	VMX: 4.4	VMX: 2.65		
SRAM-1	13.69	0	15	6	VME: 0.62	VMX: 2.3		
SI/O1		31	21	20	VME: 3.13	VMX: 0.52		
Total System					VME: 13.65			
					VMX: 4.4			
Grand Total					18.05	9.85	45%	
Total System (Data Access)					VME: 19.00			
					VMX: 5.50			
Total ICs Replaced: 72								

At Output

At End of Bus

Ch. 1 = 4.000 volts/div

Ch. 2 = 4.000 volts/div

Timebase = 20.0 ns/div

Ch. 1 Parameters

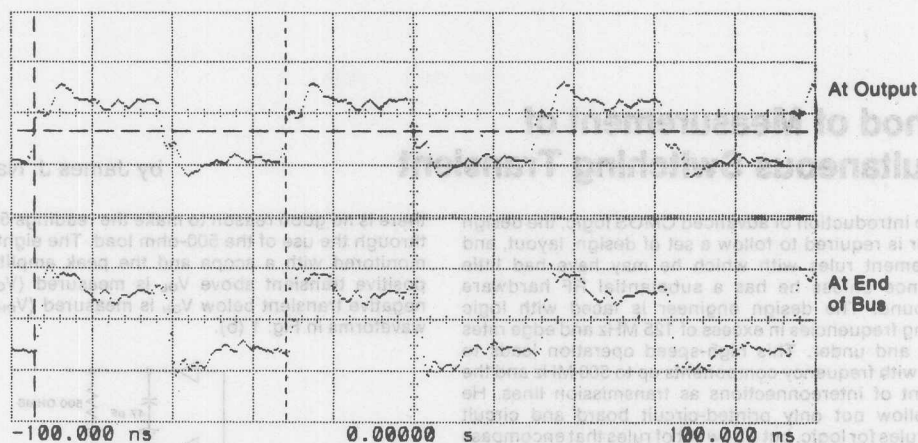
Offset = 4.000 volts

Offset = 2.800 volts

Delay = 0.00000 s

Freq. = 15.9642 MHz

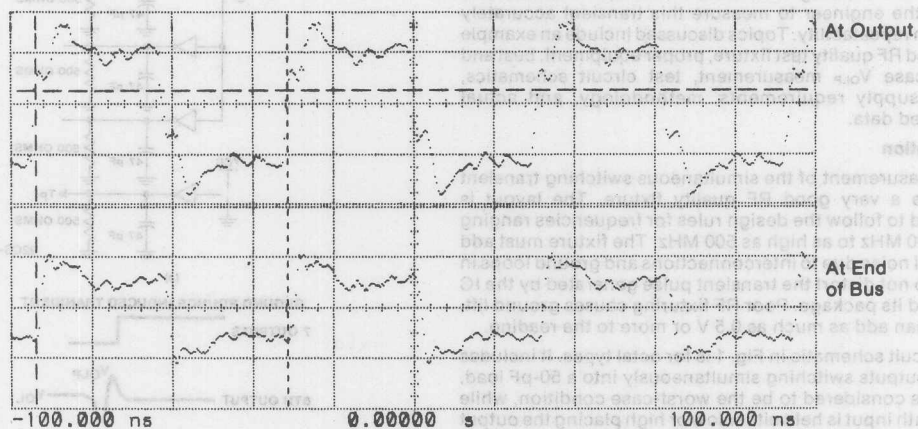
## ICAN-8640



Ch. 1 = 4.000 volts/div  
 Ch. 2 = 4.000 volts/div  
 Timebase = 20.0 ns/div  
 Ch. 1 Parameters

Offset = 4.000 volts  
 Offset = 2.800 volts  
 Delay = 0.00000 s  
 Freq. = 15.9668 MHz

Fig. 9 - Signal reflections, 2 cards.



Ch. 1 = 2.000 volts/div  
 Ch. 2 = 4.000 volts/div  
 Timebase = 20.0 ns/div  
 Ch. 1 Parameters

Offset = 2.760 volts  
 Offset = 2.800 volts  
 Delay = 0.00000 s  
 Freq. = 16.0359 MHz

Fig. 10 - Signal reflections, 1 card.

## ICAN-8754

## Method of Measurement of Simultaneous Switching Transient

by James J. Nadolski

With the introduction of advanced CMOS logic, the design engineer is required to follow a set of design, layout, and measurement rules with which he may have had little experience unless he has a substantial RF hardware background. The design engineer is faced with logic operating frequencies in excess of 125 MHz and edge rates of 5 ns and under. This high-speed operation leads to dealing with frequency components up to 500 MHz and the treatment of interconnections as transmission lines. He must follow not only printed-circuit board and circuit design rules for logic, but a new set of rules that encompass logic, RF, ECL, and analog technologies. He must also be aware of the hazards of RFI and switching noise that can occur in his design. These considerations are seldom taught in school; they are learned primarily through experience. The intent of this note is to guide the design engineer in the preferred method of measurement of the simultaneous switching transient, which also goes by the name "ground bounce effect". This measurement is difficult for accuracy and repeatability because it is an RF type of a measurement and many variables come into play that are masked in logic systems of lower speed and longer transition time. The following information and test methods will permit the engineer to measure this transient accurately and with repeatability. Topics discussed include an example of a good RF quality test fixture, proper equipment, best and worst case  $V_{OLP}$  measurement, test circuit schematics, power supply requirements, methodology, and actual measured data.

### Preparation

The measurement of the simultaneous switching transient requires a very good RF quality fixture. The layout is required to follow the design rules for frequencies ranging from 100 MHz to as high as 500 MHz. The fixture must add minimal noise due to interconnections and ground loops in order to not distort the transient pulse generated by the IC chip and its package. Poor RF fixturing causes ground lift, which can add as much as 0.5 V or more to the reading.

The circuit schematic in Fig. 1 is for octal types. It includes seven outputs switching simultaneously into a 50-pF load, which is considered to be the worst-case condition, while the eighth input is held either low or high placing the output into a high or low state, respectively. This test circuit (50 pF + 500 ohm) is the AC/ACT industry standardized AC test load. The 47-pF capacitor allows for 3 pF of additional capacitance to be contributed by the scope probe or coaxial connections. GE/RCA testing for "ground bounce" or  $V_{OLP}$  is performed for the worst-case conditions without the 500-ohm load that discharges some of the stored capacitor energy externally and not through the IC ground return path, which is significant. Inclusion of the 500-ohm resistor would unnecessarily decrease the maximum  $V_{OLP}$  reading by about 50 mV. Because CMOS inputs are purely capacitive,

there is no good reason to make the readings 50 mV lower through the use of the 500-ohm load. The eighth output is monitored with a scope and the peak amplitude of the positive transient above  $V_{OL}$  is measured ( $V_{OLP}$ ); or the negative transient below  $V_{OH}$  is measured ( $V_{OHV}$ ). See the waveforms in Fig. 1 (b).

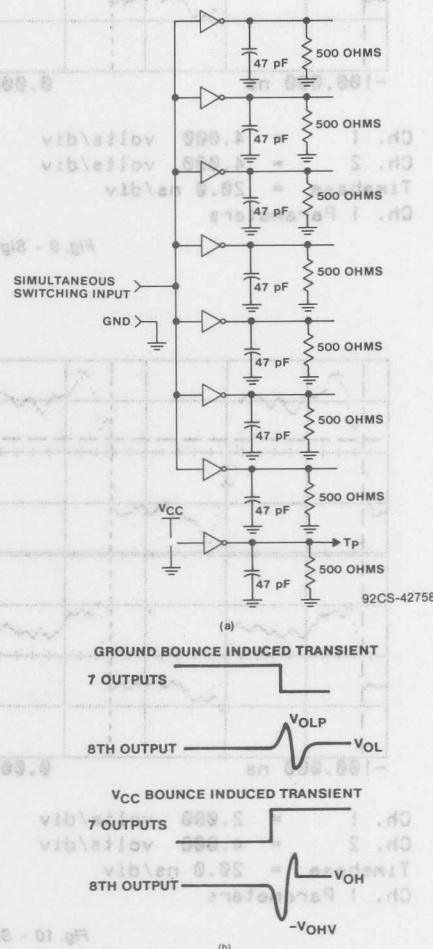


Fig. 1 - Test circuit and waveforms of simultaneous switching transient (ground bounce).

The major concern of the design engineer is the  $V_{OLP}$  or low output level. Tolerance of this noise voltage is highly dependent on the switching threshold and noise margin of the logic circuits connected to the output of the device. With the CMOS switching threshold (typically 50% of  $V_{CC}$ ) there is usually not enough energy in this pulse to cause false switching. More critical is when the logic inputs connected to the device switch at TTL thresholds (typically 1.5 V). Consequently, in order to generate  $V_{OLP}$  data as accurately as feasible, deletion of the 500-ohm external capacitor discharge load is recommended.

### Fixture Layout and Design

The fixture used in the testing of "ground bounce" is designed to be as simple and low cost as possible but follows some elementary RF rules. The printed circuit board (PCB) is double-sided glass epoxy made of FR-4 material, 2-ounce copper, with no solder mask. At these frequencies the solder mask could add leakage paths to the PCB. One side of the PCB is primarily ground plane; the other side handles the very short connections from the IC pins to the load capacitors. The value of the load capacitors is 47 pF. The total load capacitance per output is 47 pF plus 3 pF of stray capacitance for a total of 50 pF. The capacitors should be either the monolithic ceramic type with very short leads or chip capacitors. If 500-ohm resistors are also used, chip resistors are recommended. The layout of the PCB is shown in Fig. 2.

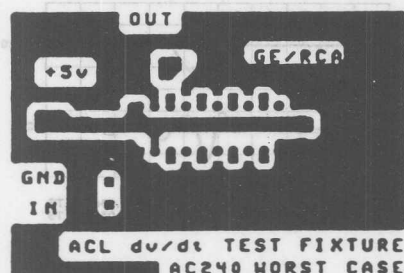


Fig. 2 - Physical layout of PCB test fixture.

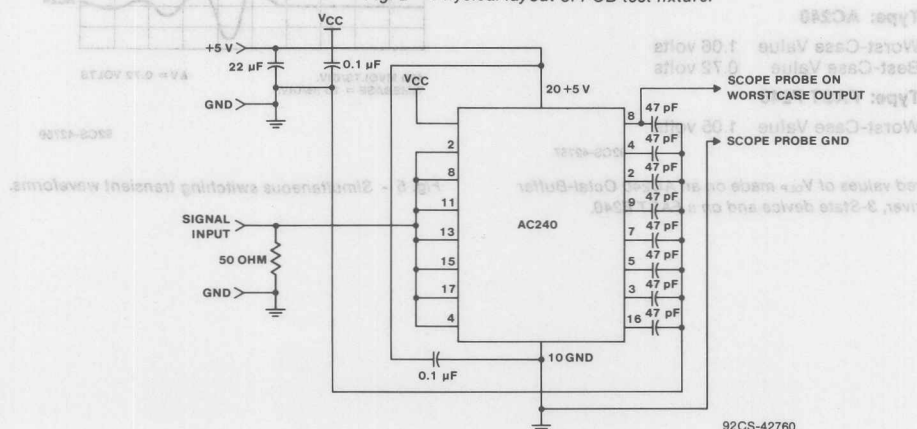


Fig. 3 - Schematic of ground bounce test circuit (worst-case condition).



jack referenced to the ground pin of the IC and the tip of the probe right at the output pin. This arrangement avoids any ground loop effects. If the proper probe is not available, the use of direct connections to the scope through a 50-ohm coaxial cable in series with a 450-ohm resistor is an alternative technique providing correlation within about 50 mV. The reduced loading of the 10000-ohm, 2-pF probe is considered more "real world" for high-impedance CMOS transient environments.

#### Equipment Required and Setup

1. The power supply must have good transient regulation so that the supply rails do not move around during switching. The supply should have added bypass capacitance at its output terminals of 1000  $\mu$ F in parallel with a 0.1- $\mu$ F ceramic disk to prevent any added ground bounce resulting from poor supply regulation.
2. The pulse generator should have a 50-ohm output and a rise and fall time of under 3 ns measured at the input of the device under test in place. The switching test frequency is set to 1-MHz output frequency.
3. The scope bandwidth should be at least 750 MHz and active probes with a similar bandwidth specification are required because of the edge rates.
4. A digital voltmeter with resolution down to 10 mV should be used to monitor the power supply voltage set for the reading.
5. A digital thermometer should be used to record the ambient temperature at the time of reading. The reading of ground bounce changes with temperature because the gain of MOS ICs changes with temperature.

#### Measurement Technique

The power supply, oscilloscope, pulse generator, and the meters should follow this warm-up procedure.

1. To allow for any drift, turn on the power supply at least one-half hour before the reading is taken.
2. Set the pulse generator output to a 1-MHz, 5-V output into a 50-ohm load.
3. With the pulse generator connected to the fixture and the test IC in place, adjust the rise and fall time to 3 ns or less.
4. Measure and record the ground bounce due to the PCB alone.

#### Type: AC240

Worst-Case Value 1.06 volts  
Best-Case Value 0.72 volts

#### Type: FAST F240

Worst-Case Value 1.05 volts

Fig. 4 - Measured values of  $V_{OLP}$  made on an AC240 Octal-Buffer Line Driver, 3-State device and on a FAST F240.

A good PCB from the standpoint of ground bounce should have a bounce voltage of under 100 mV measured directly at the IC ground return pin. The actual ground bounce effect, measured at the 8th output pin under test, includes this PCB ground bounce component.

All measurements of ground bounce used for comparison purposes should be taken under the same conditions; the power supply voltage, pulse generator frequency and transition time should be identical. The ambient temperature should be identical within 3 degrees C because logic speeds and RF leakage change with temperature.

#### Example Measurements

Fig. 4 gives results of ground bounce tests made on Advanced CMOS Logic types using the above fixture and methods. Tests were run on both the best-case output pin (closest to the IC's ground pin) and the worst-case output pin (the pin furthest from the ground pin). A comparison with a FAST 240's worst-case output pin was also made. Fig. 5 shows these results in detail as displayed on the oscilloscope.

It should be noted that the measurement of ground bounce is a difficult and time-consuming task, but accurate and reliable measurements can be made by following the above recommendations. Differences in the readings from IC to IC can be  $\pm 200$  mV. Any comparison of IC's should take this variation into consideration.

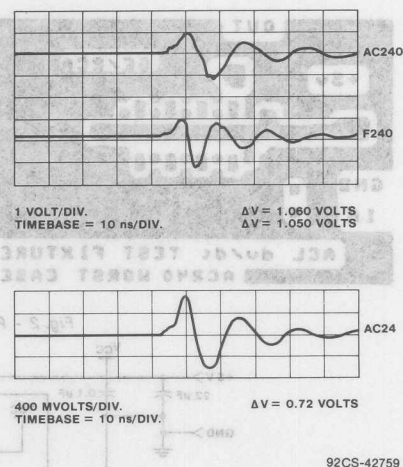
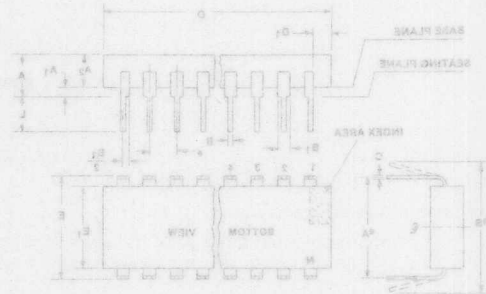


Fig. 5 - Simultaneous switching transient waveforms.



## Dual-In-Line Plastic Packages



(E) Suffix (JEDEC MS-001-AC)  
14-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES	
	MIN.	MAX.
A	—	0.210
A <sub>1</sub>	0.015	—
A <sub>2</sub>	0.115	0.195
B	0.014	0.035
B <sub>1</sub>	0.045	0.070
C	0.008	0.015
D	0.735	0.795
D <sub>1</sub>	0.005	—
E	0.300	0.325
E <sub>1</sub>	0.240	0.285
F	0.100	0.160
F <sub>1</sub>	0.115	—
G	—	0.430
H	—	0.490
I	—	0.550
J	—	0.610
K	—	0.670
L	—	0.730
M	—	0.790

93CS-38901

(E) Suffix (JEDEC MS-001-AA)  
18-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES	
	MIN.	MAX.
A	—	0.210
A <sub>1</sub>	0.015	—
A <sub>2</sub>	0.115	0.195
B	0.014	0.035
B <sub>1</sub>	0.045	0.070
C	0.008	0.015
D	0.735	0.795
D <sub>1</sub>	0.005	—
E	0.300	0.325
E <sub>1</sub>	0.240	0.285
F	0.100	0.160
F <sub>1</sub>	0.115	—
G	—	0.430
H	—	0.490
I	—	0.550
J	—	0.610
K	—	0.670
L	—	0.730
M	—	0.790

93CS-38902

(E) Suffix (JEDEC MS-001-AB)  
20-Lead Dual-In-Line Plastic Package

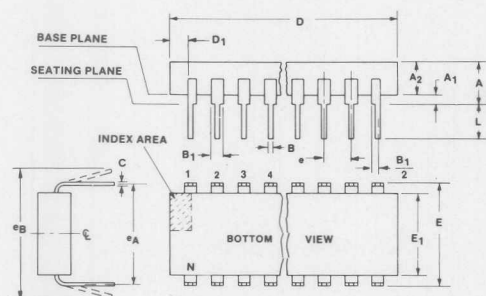
SYMBOL	INCHES	
	MIN.	MAX.
A	—	0.210
A <sub>1</sub>	0.015	—
A <sub>2</sub>	0.115	0.195
B	0.014	0.035
B <sub>1</sub>	0.045	0.070
C	0.008	0.015
D	0.735	0.795
D <sub>1</sub>	0.005	—
E	0.300	0.325
E <sub>1</sub>	0.240	0.285
F	0.100	0.160
F <sub>1</sub>	0.115	—
G	—	0.430
H	—	0.490
I	—	0.550
J	—	0.610
K	—	0.670
L	—	0.730
M	—	0.790

93CS-38903

- Notes:
1. Refer to JEDEC Publication No. 93 JEDEC Registered and Standard Outlines for Solid State Products for rules and general information concerning registered and standard outlines in Section 2.3.
  2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
  3. The dimension shown is for full leads. "Half" leads are optional at lead positions  $\frac{1}{2}N, \frac{1}{2}N+1, \dots, \frac{1}{2}N, \frac{1}{2}N+1$ .
  4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
  5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
  6. Dimension E<sub>1</sub> does not include mold flash or protrusions. E<sub>1</sub> shall be symmetrical around the center of the package.
  7. Lead spacing shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
  8. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge. (JEDEC Outline No. 93-8, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension A<sub>2</sub>.
  9. D<sub>1</sub> is the dimension to the outside of the leads and is measured at the lead tip before the device is installed. Negative lead spread is not permitted.
  10. M is the maximum number of lead positions.
  11. Dimension D<sub>1</sub> at the left end of the package must equal dimension D<sub>1</sub> at the right end of the package within 0.020 in. (0.75 mm).
  12. Pointed or rounded lead tips are permitted to ease insertion.
  13. For automatic insertion, any raised irregularity on the top surface (step, mark, etc.) shall be symmetrical about the lateral and longitudinal package centerline.

## Dimensional Outlines

## Dual-In-Line Plastic Packages



(E) Suffix (JEDEC MS-001-AC)  
14-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A <sub>1</sub>	0.015	—	0.39	—	9
A <sub>2</sub>	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B <sub>1</sub>	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	4
D <sub>1</sub>	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E <sub>1</sub>	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e <sub>A</sub>	0.300 BSC		7.62 BSC		9
e <sub>B</sub>	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	14		14		11

92CS-39901

(E) Suffix (JEDEC MS-001-AA)  
16-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A <sub>1</sub>	0.015	—	0.39	—	9
A <sub>2</sub>	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B <sub>1</sub>	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	4
D <sub>1</sub>	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E <sub>1</sub>	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e <sub>A</sub>	0.300 BSC		7.62 BSC		9
e <sub>B</sub>	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

92CS-39900

## Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions  

$$1, N, \frac{N}{2}, \frac{N}{2} + 1.$$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E<sub>1</sub> does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e<sub>A</sub>.
10. e<sub>B</sub> is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D<sub>1</sub> at the left end of the package must equal dimension D<sub>1</sub> at the right end of the package within 0.030 in. (0.76 mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

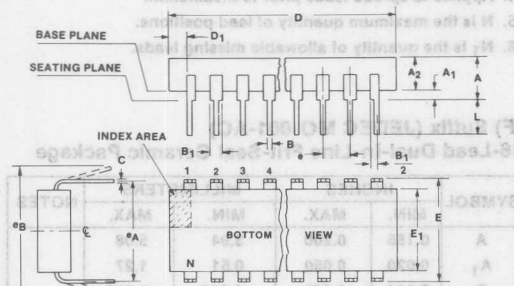
(E) Suffix (JEDEC MS-001-AE)  
20-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A <sub>1</sub>	0.015	—	0.39	—	9
A <sub>2</sub>	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B <sub>1</sub>	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.5	26.9	4
D <sub>1</sub>	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E <sub>1</sub>	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e <sub>A</sub>	0.300 BSC		7.62 BSC		9
e <sub>B</sub>	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	20		20		11

92CS-39997

# Dual-In-Line Plastic Packages

## (EN) Suffix (JEDEC MS-001-AF) 24-Lead Dual-In-Line Plastic Package



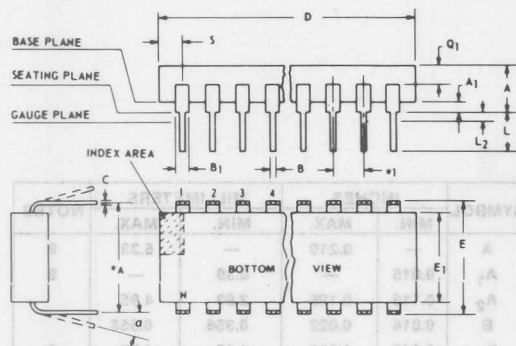
### Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions  $\frac{N}{2} - 1$  and  $\frac{N}{2}$ .
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A <sub>1</sub>	0.015	—	0.39	—	9
A <sub>2</sub>	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B <sub>1</sub>	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.6	32.3	4
D <sub>1</sub>	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E <sub>1</sub>	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e <sub>A</sub>	0.300 BSC		7.62 BSC		9
e <sub>B</sub>	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	24		24		11

92CS-39943

8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e<sub>A</sub>.
10. e<sub>B</sub> is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D<sub>1</sub> at the left end of the package must equal dimension D<sub>1</sub> at the right end of the package within 0.030 in. (0.76 mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.



(F) Suffix (JEDEC MO-001-AB)  
14-Lead Dual-In-Line Frit-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.155	0.200	3.94	5.08	
A <sub>1</sub>	0.020	0.050	0.51	1.27	
B	0.014	0.020	0.356	0.508	
B <sub>1</sub>	0.050	0.065	1.27	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.745	0.770	18.93	19.55	
E	0.300	0.325	7.62	8.25	
E <sub>1</sub>	0.240	0.260	6.10	6.60	
e <sub>1</sub>	0.100 TP		2.54 TP		2
e <sub>A</sub>	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	
L <sub>2</sub>	0.000	0.030	0.00	0.76	
a	0°	15°	0°	15°	4
N	14		14		5
N <sub>1</sub>	0		0		6
Q <sub>1</sub>	0.040	0.075	1.02	1.90	
S	0.065	0.090	1.66	2.28	

92SS-4296R3

(F) Suffix  
20-Lead Dual-In-Line Frit-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.120	0.250	3.10	6.30	
A <sub>1</sub>	0.020	0.070	0.51	1.77	
B	0.016	0.020	0.407	0.508	
B <sub>1</sub>	0.028	0.070	0.72	1.77	
C	0.008	0.012	0.204	0.304	1
D	0.942	0.990	23.93	25.15	
E	0.300	0.325	7.62	8.25	
E <sub>1</sub>	0.240	0.280	6.10	7.11	
e <sub>1</sub>	0.100 TP		2.54 TP		2
e <sub>A</sub>	0.300 TP		7.62 TP		2, 3
L	0.100	0.200	2.54	5.00	
L <sub>2</sub>	0.000	0.030	0.00	0.76	
α	0° C	15° C	0° C	15° C	4
N	20		20		5
N <sub>1</sub>	0		0		6
Q <sub>1</sub>	0.040	0.075	1.02	1.90	
S	0.040	0.100	1.02	2.54	

92CM-35137R1

# NOTES:

Refer to JEDEC Publication No. 95 for Rules for Dimensioning Axial Lead Product Outlines.

- When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 in. (0.33 mm).
- Leads within 0.005 in. (0.127 mm) radius of True Position (TP) at gauge plane with maximum material condition.
- e<sub>A</sub> applies in zone L<sub>2</sub> when unit is installed.
- Applies to spread leads prior to installation.
- N is the maximum quantity of lead positions.
- N<sub>1</sub> is the quantity of allowable missing leads.

(F) Suffix (JEDEC MO-001-AC)  
16-Lead Dual-In-Line Frit-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.155	0.200	3.94	5.08	
A <sub>1</sub>	0.020	0.050	0.51	1.27	
B	0.014	0.020	0.356	0.508	
B <sub>1</sub>	0.035	0.065	0.89	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.745	0.785	18.93	19.93	
E	0.300	0.325	7.62	8.25	
E <sub>1</sub>	0.240	0.260	6.10	6.60	
e <sub>1</sub>	0.100 TP		2.54 TP		2
e <sub>A</sub>	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	
L <sub>2</sub>	0.000	0.030	0.00	0.76	
a	0°	15°	0°	15°	4
N	16		16		5
N <sub>1</sub>	0		0		6
Q <sub>1</sub>	0.040	0.075	1.02	1.90	
S	0.015	0.060	0.39	1.52	

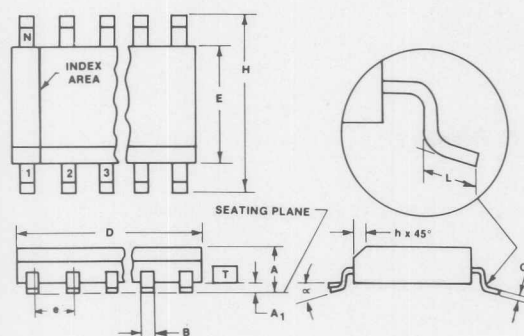
92CM-15967R4

(F) Suffix (JEDEC MO-015-AA)  
24-Lead Dual-In-Line Frit-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.120	0.250	3.10	6.30	
A <sub>1</sub>	0.020	0.070	0.51	1.77	
B	0.016	0.020	0.407	0.508	
B <sub>1</sub>	0.028	0.070	0.72	1.77	
C	0.008	0.012	0.204	0.304	1
D	1.200	1.290	30.48	32.76	
E	0.600	0.625	15.24	15.87	
E <sub>1</sub>	0.515	0.580	13.09	14.73	
e <sub>1</sub>	0.100 TP		2.54 TP		2
e <sub>A</sub>	0.600 TP		15.24 TP		2, 3
L	0.100	0.200	2.54	5.00	
L <sub>2</sub>	0.000	0.030	0.00	0.76	
α	0° C	15° C	0° C	15° C	4
N	24		24		5
N <sub>1</sub>	0		0		6
Q <sub>1</sub>	0.040	0.075	1.02	1.90	
S	0.040	0.100	1.02	2.54	

92CS-26938R3

## Dual-In-Line Small-Outline Plastic Packages



## NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "T" is a reference datum.
4. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

## (M) Suffix (JEDEC MS-012-AB)

## 14-Lead Dual-In-Line Small-Outline Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A <sub>1</sub>	0.0040	0.0098	0.10	0.25	
B	0.0138	0.0192	0.35	0.49	
C	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38924R1

## (M) Suffix (JEDEC MS-012-AC)

## 16-Lead Dual-In-Line Small-Outline Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A <sub>1</sub>	0.0040	0.0098	0.10	0.25	
B	0.0138	0.0192	0.35	0.49	
C	0.0075	0.0098	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38925R1

## (M) Suffix (JEDEC MS-013-AC)

## 20-Lead Dual-In-Line Small-Outline Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A <sub>1</sub>	0.0040	0.0118	0.10	0.30	
B	0.0138	0.0192	0.35	0.49	
C	0.0091	0.0125	0.23	0.32	
D	0.4961	0.5118	12.60	13.00	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38926R1

## (M) Suffix (JEDEC MS-013-AD)

## 24-Lead Dual-In-Line Small-Outline Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A <sub>1</sub>	0.0040	0.0118	0.10	0.30	
B	0.0138	0.0192	0.35	0.49	
C	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

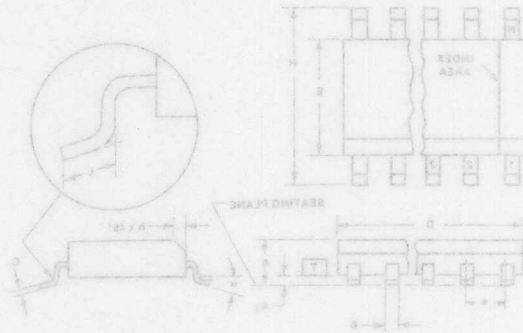
92CS-39037R1



# Dual-In-Line Small-Outline Plastic Packages

## NOTES

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1992.
3. "T" is a reference datum.
4. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.005 in.).
5. The diameter on the body is optional. If it is not present, a visual index feature must be located within the cross hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.



(M) Suffix (JEDEC MS-013-AD)  
16-Lead Dual-In-Line Small-Outline Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0082	0.0088	0.208	0.224	
A <sub>1</sub>	0.0040	0.0046	0.102	0.118	
B	0.0138	0.0142	0.350	0.361	
C	0.0072	0.0078	0.183	0.198	
D	0.0082	0.0087	0.208	0.221	
E	0.0087	0.0092	0.221	0.234	
e	0.000 BSC		0.000 BSC		
H	0.0084	0.0090	0.214	0.229	
H <sub>1</sub>	0.0039	0.0045	0.100	0.114	
L	0.018	0.020	0.457	0.508	
N	0	16	0	16	

Notes: 1, 2, 3, 8, 9

(M) Suffix (JEDEC MS-013-AB)  
14-Lead Dual-In-Line Small-Outline Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0082	0.0088	0.208	0.224	
A <sub>1</sub>	0.0040	0.0046	0.102	0.118	
B	0.0138	0.0142	0.350	0.361	
C	0.0072	0.0078	0.183	0.198	
D	0.0082	0.0087	0.208	0.221	
E	0.0087	0.0092	0.221	0.234	
e	0.000 BSC		0.000 BSC		
H	0.0084	0.0090	0.214	0.229	
H <sub>1</sub>	0.0039	0.0045	0.100	0.114	
L	0.018	0.020	0.457	0.508	
N	0	14	0	14	

Notes: 1, 2, 3, 8, 9

(M) Suffix (JEDEC MS-013-AD)  
24-Lead Dual-In-Line Small-Outline Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0082	0.0088	0.208	0.224	
A <sub>1</sub>	0.0040	0.0046	0.102	0.118	
B	0.0138	0.0142	0.350	0.361	
C	0.0072	0.0078	0.183	0.198	
D	0.0082	0.0087	0.208	0.221	
E	0.0087	0.0092	0.221	0.234	
e	0.000 BSC		0.000 BSC		
H	0.0084	0.0090	0.214	0.229	
H <sub>1</sub>	0.0039	0.0045	0.100	0.114	
L	0.018	0.020	0.457	0.508	
N	0	24	0	24	

Notes: 1, 2, 3, 8, 9

(M) Suffix (JEDEC MS-013-AC)  
20-Lead Dual-In-Line Small-Outline Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0082	0.0088	0.208	0.224	
A <sub>1</sub>	0.0040	0.0046	0.102	0.118	
B	0.0138	0.0142	0.350	0.361	
C	0.0072	0.0078	0.183	0.198	
D	0.0082	0.0087	0.208	0.221	
E	0.0087	0.0092	0.221	0.234	
e	0.000 BSC		0.000 BSC		
H	0.0084	0.0090	0.214	0.229	
H <sub>1</sub>	0.0039	0.0045	0.100	0.114	
L	0.018	0.020	0.457	0.508	
N	0	20	0	20	

Notes: 1, 2, 3, 8, 9